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## Notes on Using the E200F Emulator --R0E0200F1EMU00-- for the SH-2- and SH-2A-Cored CPUs

Please take note of the four problems described below in using the E200F emulator--R0E0200F1EMU00--for the SH-2- and SH-2A-cored CPUs.

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### 1. Product and Versions Concerned

The E200F emulator R0E0200F1EMU00

Version V.1.00 Release 00 through V.2.01 Release 01

(for the SH7206 group, SH7200 series; and SH7211 group, SH7210 series, SuperH RISC engine family of MCUs)

### 2. Problems

#### 2.1 Problem 1

When a member of the SH7206 group, SH7200 device series is used as the target CPU, the program may not be halted at the specified software breakpoint at the second time.

This problem occurs if you go through the following steps:

- (1) The program is executed with the CPU's cache function valid.
- (2) After the program is once halted at a software breakpoint A, for example, it is re-executed with the breakpoint A established.
- (3) The program again reaches the breakpoint A without being halted at any software breakpoint other than A. (This time, the program may not be halted.)

Workaround:

Establish two or more breakpoints in order that the program might not reach the

same breakpoint successively.

## 2.2 Problem 2

When a member of the SH7211 group, SH7210 device series is used as the target CPU, the debugger may not be invoked.

This problem is as follows:

If you invoke the debugger, the Connecting dialog box automatically opens. While "Downloading firmware" is being displayed in this dialog box, a Time out error may arise, causing the debugger not to be normally launched.

Workaround:

If a Time out error arises, restart the debugger.

## 2.3 Problem 3

When the SH7211F, SH7206 group, SH7200 device series is used as the target CPU, the Wave register appears in the I/O Register window.

The appearance of the Wave register, though it should not be in the SH7211F, does not affect any debug operations. But don't use the Wave register.

## 2.4 Problem 4

When an SoC using a member of the SH7206 group, SH7200 device series; the SH7211 group, SH7210 device series; or the SH-2A core is the target CPU, the emulation memory (optional) may not be accessed.

This problem occurs if the following conditions are both satisfied:

- (1) Though selected in the user system, the RD/WR pin is not selected using the pin function controller (PFC) in the user program and the emulator software.
- (2) Memory in the emulation memory unit R0E0200F1MSR00 or R0E0200F1MSR01 is used.

Workaround:

When the RD/WR pin is used in the user system, select this pin in the user program and the emulator software using the pin function controller (PFC).

## 3. Schedule of Fixing the Problems

We plan to fix these programs in the next release of the product.

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