Outline

When using the product in the title, note the following point.

1. Selecting the PLL circuit as the CLKOUT pin’s output clock source in the RX140 CLKOUT output function.

1. Selecting the PLL circuit as the CLKOUT pin’s output clock source in the RX140 CLKOUT output function

1.1 Applicable Products

(1) Board Support Package Module Using Firmware Integration Technology (BSP FIT Module)

The applicable revision and document are as follows.

<table>
<thead>
<tr>
<th>Revision</th>
<th>Document number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev.6.20</td>
<td>R01AN1685EJ0620</td>
</tr>
</tbody>
</table>

1.2 Applicable Devices

- RX140 group

1.3 Details

The oscillation of the PLL circuit is not executed properly under certain conditions.

If an option other than the PLL circuit is selected as the clock source (BSP_CFG_CLOCK_SOURCE ≠ 4) and the PLL circuit as the CLKOUT pin’s output clock source (BSP_CFG_CLKOUT_SOURCE = 4), the oscillation of the PLL circuit is disabled. Therefore, the CLKOUT pin does not output the PLL clock.

1.4 Conditions

The problem arises if the following conditions are met.

(1) RX140 is selected for the device.

(2) In Smart Configurator, an option other than the PLL circuit is selected as the clock source (BSP_CFG_CLOCK_SOURCE ≠ 4), and the PLL circuit as the CLKOUT clock source (BSP_CFG_CLKOUT_SOURCE = 4). Check the checkbox of the CLKOUT pin output and start generating codes.
1.5 Workaround
Refer to the following and modify mcuxr140mcu_clocks.c as shown in red.

clock_source_select() (L546 to L564)
Before modification

```c
#if BSP_CFG_CLOCK_SOURCE == 4
   /* PLL is chosen. Start it operating if it is not already. Must start main clock as well since PLL
    uses it. */

   /* Set PLL Input Divisor. */
   SYSTEM.PLLCR.BIT.PLIDIV = BSP_CFG_PLL_DIV >> 1;

   /* Set PLL Multiplier. */
   SYSTEM.PLLCR.BIT.STC  = (BSP_CFG_PLL_MUL * 2) - 1;

   /* Set the PLL to operating. */
   SYSTEM.PLLCR2.BYTE = 0x00;

   /* WAIT_LOOP */
   while (0 == SYSTEM.OSCOVFSR.BIT.PLOVF)
   {
      /* Make sure clock has stabilized. */
      R_BSP_NOP();
   }
#endif
```
After modification

```c
#if BSP_PRV_PLL_CLK_OPERATING == 1
  /* PLL is chosen. Start it operating if it is not already. Must start main clock as well since PLL
  uses it. */

  /* Set PLL Input Divisor. */
  SYSTEM.PLLCR.BIT.PLIDIV = BSP_CFG_PLL_DIV >> 1;

  /* Set PLL Multiplier. */
  SYSTEM.PLLCR.BIT.STC = (BSP_CFG_PLL_MUL * 2) - 1;

  /* Set the PLL to operating. */
  SYSTEM.PLLCR2.BYTE = 0x00;

  /* WAIT_LOOP */
  while (0 == SYSTEM.OSCOVFSR.BIT.PLOVF)
  {
    /* Make sure clock has stabilized. */
    R_BSP_NOP();
  }
#endif
```

1.6 Schedule for Fixing the Problem

The problem is fixed in BSP Rev.6.21 (document number: R01AN1685EJ0621). Update your product to BSP Rev.6.21.
Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Oct.01.21</td>
<td>-</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

The past news contents have been based on information at the time of publication. Now changed or invalid information may be included.

The URLs in the Tool News also may be subject to change or become invalid without prior notice.

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/