[Notes]
CS+ Smart Configurator for RX,
e^2 studio Smart Configurator Plug-in

R20TS0294EJ0100
Rev.1.00
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Outline

When using the products in the title, note the following point.

1. When using the bus for peripheral functions

1. When Using the Bus for Peripheral Functions

1.1 Applicable Products

- CS+ Smart Configurator for RX V1.3.0
- e^2 studio V6.2.0 (Smart Configurator Plug-in)

1.2 Applicable MCUs

- RX family: RX230 and RX231 groups

1.3 Details

When an external bus is specified to be used in the products listed in section 1.2, associated address output enable registers 0 and 1 (PFAOE0 and PFAOE1) are set incorrectly. As a result, the pins for the following peripheral functions (which also function as the pins for the external bus) become unavailable even though the corresponding bits are disabled for the external bus. See Table 1 for the peripheral function pins that also function as the pins for the external bus.

- Peripheral functions that are affected as a result of the external bus being used
  - Multi-function timer pulse unit 2 (MTU2a)
  - 8-bit timer (TMR)
  - 16-bit timer pulse unit (TPUa)
  - Port output enable (POE2a)
  - Serial communications interfaces (SCIg, SCIh)
  - Serial peripheral interface (RSPIa)
  - IrDA interface
  - USB 2.0 host/function module (USBd)
  - Clock frequency accuracy measurement circuit (CAC)
  - SD host interface (SDHIa)
  - Capacitive touch sensing unit (CTSU)
  - Interrupt controller (ICUb)
  - Comparator B (CMPBa)

Table 1 Pins That Are Used as I/O Pins for the External Bus and as Pins for Peripheral Functions

Pin Name	External Bus Pin	MTU	TMR	POE	TPU
PC7	A23/CS0#	MTIOC3A(MTU3)/MTCLKB	TMO2(TMR2)		
PC6	A22/CS1#	MTIOC3C(MTU3)/MTCLKA	TMCI2(TMR2)		
PC5	A21/CS2#/WAIT#	MTIOC3B(MTU3)/MTCLKD	TMRI2(TMR2)		
PC4	A20/CS3#	MTIOC3D(MTU3)/MTCLKC	TMCI1(TMR1)	POE0#(POE)	
PC3	A19	MTIOC4D(MTU4)			TCLKB
PC2	A18	MTIOC4B(MTU4)			TCLKA
PC1	A17	MTIOC3A(MTU3)			TCLKD
PC0	A16	MTIOC3C(MTU3)			TCLKC
PB7	A15	MTIOC3B(MTU3)			TIOCB5(TPU5)
PB6	A14	MTIOC3D(MTU3)			TIOCA5(TPU5)
PB5	A13	MTIOC2A(MTU2)/MTIOC1B(MTU1)	TMRI1(TMR1)	POE1#(POE)	TIOCB4(TPU4)
PB4	A12				TIOCA4(TPU4)
PB3	A11	MTIOC0A(MTU0)/MTIOC4A(MTU4)	TMO0(TMR0)	POE3#(POE)	TIOCD3(TPU3)/TCLKD
PB2	A10				TIOCC3(TPU3)/TCLKC
PB1	A9	MTIOC0C(MTU0)/MTIOC4C(MTU4)	TMCI0(TMR0)		TIOCB3(TPU3)
PB0	A8	MTIC5W(MTU5)			TIOCA3(TPU3)

Pin Name	External Bus Pin	SCI	RSPI	IrDA	USBd
PC7	A23/CS0#	TXD8/SMOSI8/SSDA8(SCI8)	MISOA(RSPI0)		
PC6	A22/CS1#	RXD8/SMISO8/SSCL8(SCI8)	MOSIA(RSPI0)		
PC5	A21/CS2#/WAIT#	SCK8(SCI8)	RSPCKA(RSPI0)		
PC4	A20/CS3#	SCK5(SCI5)/CTS8#/RTS8#/SS8#(SCI8)	SSLA0(RSPI0)		
PC3	A19	TXD5/SMOSI5/SSDA5(SCI5)		IRTXD5	
PC2	A18	RXD5/SMISO5/SSCL5(SCI5)	SSLA3(RSPI0)	IRRXD5	
PC1	A17	SCK5(SCI5)	SSLA2(RSPI0)		
PC0	A16	CTS5#/RTS5#/SS5#(SCI5)	SSLA1(RSPI0)		
PB7	A15	TXD9/SMOSI9/SSDA9(SCI9)			
PB6	A14	RXD9/SMISO9/SSCL9(SCI9)			
PB5	A13	SCK9(SCI9)			USB0_VBUS
PB4	A12	CTS9#/RTS9#/SS9#(SCI9)			
PB3	A11	SCK6(SCI6)			
PB2	A10	CTS6#/RTS6#/SS6#(SCI6)			
PB1	A9	TXD6/SMOSI6/SSDA6(SCI6)			
PB0	A8	RXD6/SMISO6/SSCL6(SCI6)	RSPCKA(RSPI0)		

Pin Name	External Bus Pin	CAC	SDHI	CTSU	ICU	CMPBa
PC7	A23/CS0#	CACREF				
PC6	A22/CS1#			TS22		
PC5	A21/CS2#/WAIT#			TS23		
PC4	A20/CS3#		SDHI_D1	TSCAP		
PC3	A19		SDHI_D0	TS27		
PC2	A18		SDHI_D3	TS30		
PC1	A17			TS33		
PC0	A16			TS35		
PB7	A15		SDHI_D2			
PB6	A14		SDHI_D1			
PB5	A13		SDHI_CD			
PB4	A12					
PB3	A11		SDHI_WP			
PB2	A10					
PB1	A9		SDHI_CLK		IRQ4	CMPOB1
PB0	A8		SDHI_CM			

1.4 Workaround

Use void R_Config_BSC_Create_UserInit(void) (user initialization function) to modify the settings of address output enable registers 0 and 1 (PFAOE0 and PFAOE1) to match the address output pin settings.
(1) below shows a modification example when external address bus output pins A0 to A7 are used. (2) shows a modification example when external address bus output pins A0 to A15 are used.

(1) Modification example when using address output pins A0 to A7

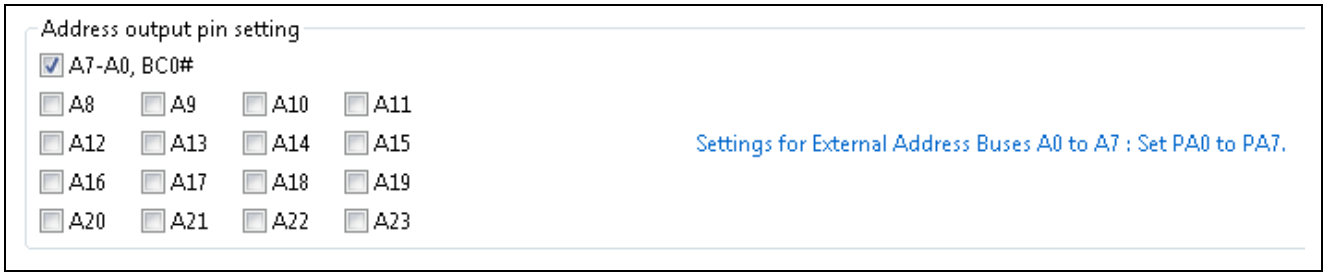

Figure 1. Smart configurator bus setting window

Use the void R_Config_BSC_Create_UserInit(void) function in Config_BSC_user.c to add code that sets the address output enable registers 0 and 1 (PFAOE0 and PFAOE1) to “0” (disable output). The modification is shown in red.

```
void R_Config_BSC_Create_UserInit(void)
{
    /* Start user code. Do not edit comment generated here */
    MPC.PFAOE0.BYTE = 0;
    MPC.PFAOE1.BYTE = 0;
    /* End user code. Do not edit comment generated here */
}
```

(2) Modification example when using address output pins A0 to A15

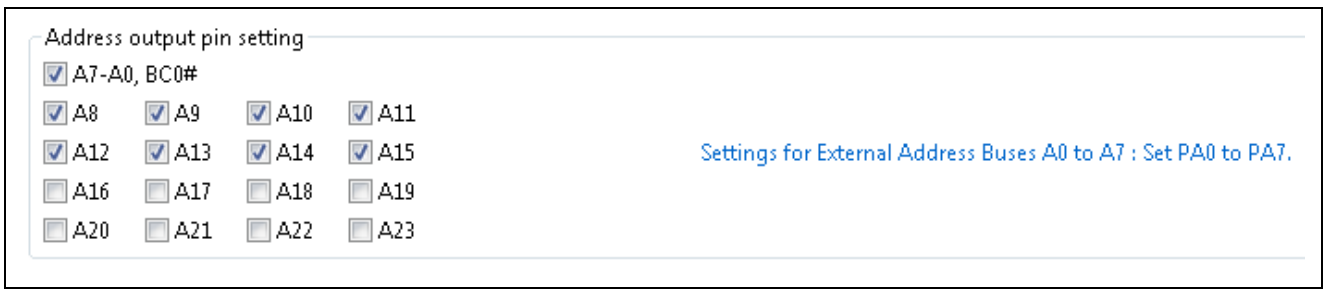

Figure 2. Smart configurator bus setting window

Use the void R_Config_BSC_Create_UserInit(void) function in Config_BSC_user.c to add code that sets the address output enable register 0 (PFAOE0) to “1” (enable output) and address output enable register 1 (PFAOE1) to “0” (disable output). The modification is shown in red.

```
void R_Config_BSC_Create_UserInit(void)
{
    /* Start user code. Do not edit comment generated here */
    MPC.PFAOE0.BYTE = 0xFF;
    MPC.PFAOE1.BYTE = 0;
    /* End user code. Do not edit comment generated here */
}
```

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version.

1.6 Reference Information

This section shows the reference information on address output enable registers 0 and 1 (PFAOE0 and PFAOE1). For details, refer to the URL below.

https://www.renesas.com/search/keyword-search.html#genre=document&q=r01uh0496

RX230 Group, RX231 Group User's Manual: Hardware

Address Output Enable Register 0 (PFAOE0)

b7	b6	b5	b4	b3	b2	b1	b0
A15E	A14E	A13E	A12E	A11E	A10E	A9E	A8E

Bit	Symbol	Bit Name	Description	R/W
b0	A8E	Address A8 Output Enable	0: Disables A8 output. 1: Enables A8 output.	R/W
b1	A9E	Address A9 Output Enable	0: Disables A9 output. 1: Enables A9 output.	R/W
b2	A10E	Address A10 Output Enable	0: Disables A10 output. 1: Enables A10 output.	R/W
b3	A11E	Address A11 Output Enable	0: Disables A11 output. 1: Enables A11 output.	R/W
b4	A12E	Address A12 Output Enable	0: Disables A12 output. 1: Enables A12 output.	R/W
b5	A13E	Address A13 Output Enable	0: Disables A13 output. 1: Enables A13 output.	R/W
b6	A14E	Address A14 Output Enable	0: Disables A14 output. 1: Enables A14 output.	R/W
b7	A15E	Address A15 Output Enable	0: Disables A15 output. 1: Enables A15 output.	R/W

The PFAOE0 register selects enabling or disabling of address output.

Address Output Enable Register 1 (PFAOE1)

b7	b6	b5	b4	b3	b2	b1	b0
A23E	A22E	A21E	A20E	A19E	A18E	A17E	A16E

Bit	Symbol	Bit Name	Description	R/W
b0	A16E	Address A16 Output Enable	0: Disables A16 output. 1: Enables A16 output.	R/W
b1	A17E	Address A17 Output Enable	0: Disables A17 output. 1: Enables A17 output.	R/W
b2	A18E	Address A18 Output Enable	0: Disables A18 output. 1: Enables A18 output.	R/W
b3	A19E	Address A19 Output Enable	0: Disables A19 output. 1: Enables A19 output.	R/W
b4	A20E	Address A20 Output Enable	0: Disables A20 output. 1: Enables A20 output.	R/W
b5	A21E	Address A21 Output Enable	0: Disables A21 output. 1: Enables A21 output.	R/W
b6	A22E	Address A22 Output Enable	0: Disables A22 output. 1: Enables A22 output.	R/W
b7	A23E	Address A23 Output Enable	0: Disables A23 output. 1: Enables A23 output.	R/W

The PFAOE1 register selects enabling or disabling of address output.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 1, 2018	-	First edition issued

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061 Japan

Renesas Electronics Corporation

■Inquiry

https://www.renesas.com/contact/