[Note]
CS+, CubeSuite+, and e^2 studio
Integrated Development Environments

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Outline

When using the CS+, CubeSuite+, or e^2 studio integrated development environment, take note of the problem described in this note regarding the following point.

1. Using an on-chip debugging emulator while the sub-system clock of certain RL78 family products is operating

1. Using an On-chip Debugging Emulator while the Sub-system Clock of Certain RL78 Family Products is Operating

1.1 Applicable Software Products

- RL78 Family C Compiler Package (with IDE)

  The version of the CS+ for CC common program is V3.00.00 or later.

- RL78 and 78K Family C Compiler Package (with IDE)

  The version of the CS+ for CA, CX common program is V3.00.00 or later, or the version of the CubeSuite+ common program is V2.02.00 or later.

- [Evaluation edition] Integrated Development Environment CS+ for CC

  The version of the CS+ for CC common program is V3.00.00 or later.

- [Evaluation edition] Integrated Development Environment CS+ for CA, CX

  The version of the CS+ for CA, CX common program is V3.00.00 or later.

- [Evaluation edition] Integrated Development Environment CubeSuite+

  The version of the CubeSuite+ common program is V2.02.00 or later.

- The version of the e^2 studio is V1.1.0 or later.

Applicable emulators: E1, E20, and E2 emulator Lite

1.2 Applicable MCUs

RL78/I1D and RL78/G1F groups

1.3 Details

After the setting “System” is made for [Monitor clock] in [Clock] on the [Connect Settings] tab of the property panel of the debugging tool, a communications error may arise between the emulator and MCU so that the debugging tool does not operate correctly when a program is stopped while the sub-system clock is operating.

1.4 Conditions

This problem arises if the following conditions are all met:

(1) The setting of bit 6 (CSS) in the system clock control register (CKC) of the MCU is “1” (selecting the sub-system clock).

(2) Either of the following settings (a) or (b) is in place.

(a) The setting of bit 4 (MCM0) in the system clock control register (CKC) of the MCU is “1” (selecting the high-speed system clock as the main-system clock).

(b) The setting of bit 0 (MCM1) in the system clock control register (CKC) of the MCU is “1” (selecting the medium speed on-chip oscillator clock as the main on-chip oscillator clock).

Note: The problem does not arise when the setting of bit 4 (MCM0) in the system clock control register (CKC) is “0” (selecting the main on-chip oscillator clock as the main-system clock) and that of bit 0 (MCM1) is “0” (selecting the high speed on-chip oscillator clock as the main on-chip oscillator clock).

1.5 Workaround

Do not stop a program while the sub-system clock is operating when the setting “System” has been made for [Monitor clock] in [Clock] on the [Connect Settings] tab of the property panel of the debugging tool.

1.6 Schedule for Fixing the Problem

This problem will be fixed in the next version.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul. 16, 2016	-	First edition issued

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