[Notes]
CS+ Code Generator for RL78 (CS+ for CC),
CS+ Code Generator for RL78 (CS+ for CA, CX),
e^2 studio Code Generator Plug-in,
Applilet3 Coding Assistance Tool for RL78

R20TS0432EJ0100
Rev.1.00
Jun. 01, 2019

Outline

When using the products in the title, note the following points.

1. PLL clock setting of clock generator
2. RTC operation clock setting of clock generator

1. PLL Clock Setting of Clock Generator

1.1 Applicable Products

- CS+ Code Generator for RL78 V3.02.00 (CS+ for CC V2.05) and later
- CS+ Code Generator for RL78 V3.02.00 (CS+ for CA,CX V2.05) and later
- Code Generator Plug-in V1.0.1 (e^2 studio V2.2.0) and later
- Applilet3 for RL78 V1.01.00 and later

1.2 Applicable Devices

RL78 family: RL78/F13, RL78/F14, and RL78/F15 group

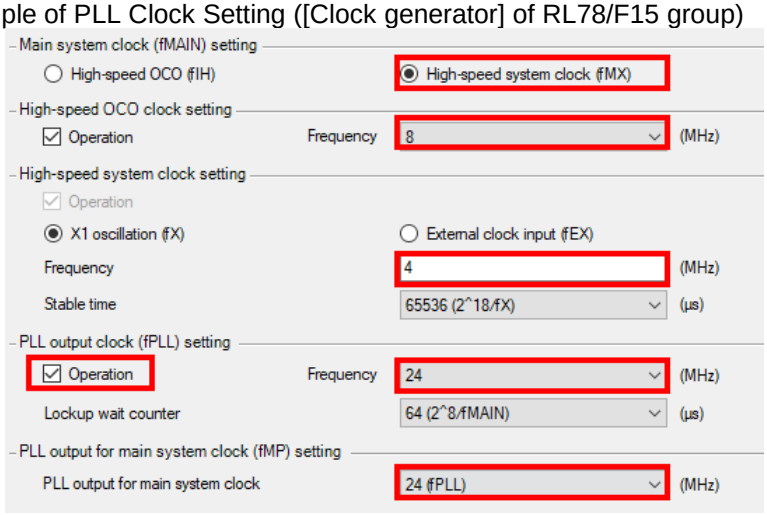
1.3 Details

When you perform the following settings in the [Clock generator] of the applicable products, the code generated for setting the division of the PLL output is incorrect. The division setting of the PLL output specifies to divide the clock frequency by 4 instead of 2, making the PLL clock (fPLL) frequency half of the intended value.

(Example: When 24MHz is selected in the PLL clock (fPLL) setting, the frequency will be half of the selected value (=12MHz).)

- Clock Generator
  - Main system clock (fMAIN)) setting > select High-speed system clock (fMX)
  - High-speed OCO clock setting > check the [Operation] checkbox and select 8MHz for the frequency
  - High-speed system clock setting > select 4MHz for the frequency
  - PLL clock (fPLL) setting > check the [Operation] checkbox and select 24MHz or 32MHz for the frequency
  - PLL output for main system clock (fMP) setting > select the same frequency as the PLL clock (fPLL) setting

➢ Example of PLL Clock Setting ([Clock generator] of RL78/F15 group)



1.4 Workaround

When you set the code generator as described in section 1.3, the PLL clock frequency (fPLL) will be half of the setting value. You will need to modify the code in the following steps to make the correct division setting of the PLL output (to divide the clock frequency by 2).
After generating code, open R_CGC_Create(void) in the r_cg_cgc.c and modify the following code written in the red box.

Note that if you perform code generation again, the modified code (above) will be overwritten. Thus, you will need to modify the code in the steps above after each code generation.

➢ Before modification

```
void R_CGC_Create(void)
{
    volatile uint32_t w_count;
    uint8_t           temp_stab_set;
    uint8_t           temp_stab_wait;

    /* Set fPLL */
    PLLCTL = _40_CGC_LOCKUP_WAIT_8 | _00_CGC_PLL_BELOW_32MHZ | _10_CGC_PLL_DIVISION_4 | _00_CGC_PLL_MULTIPLY_X12;
```

➢ After modification

```
void R_CGC_Create(void)
{
    volatile uint32_t w_count;
    uint8_t           temp_stab_set;
    uint8_t           temp_stab_wait;

    /* Set fPLL */
    PLLCTL = _40_CGC_LOCKUP_WAIT_8 | _00_CGC_PLL_BELOW_32MHZ | _00_CGC_PLL_DIVISION_2 | _00_CGC_PLL_MULTIPLY_X12;
```

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in July 2019.)

2. RTC Operation Clock Setting of Code Generator

2.1 Applicable Products

- CS+ Code Generator for RL78 V3.02.00 (CS+ for CC V2.05) and later
- CS+ Code Generator for RL78 V3.02.00 (CS+ for CA,CX V2.05) and later
- Code Generator plug-in V1.0.1 (e^2 studio V2.2.0) and later
- Applilet3 for RL78 V1.00.00 and later

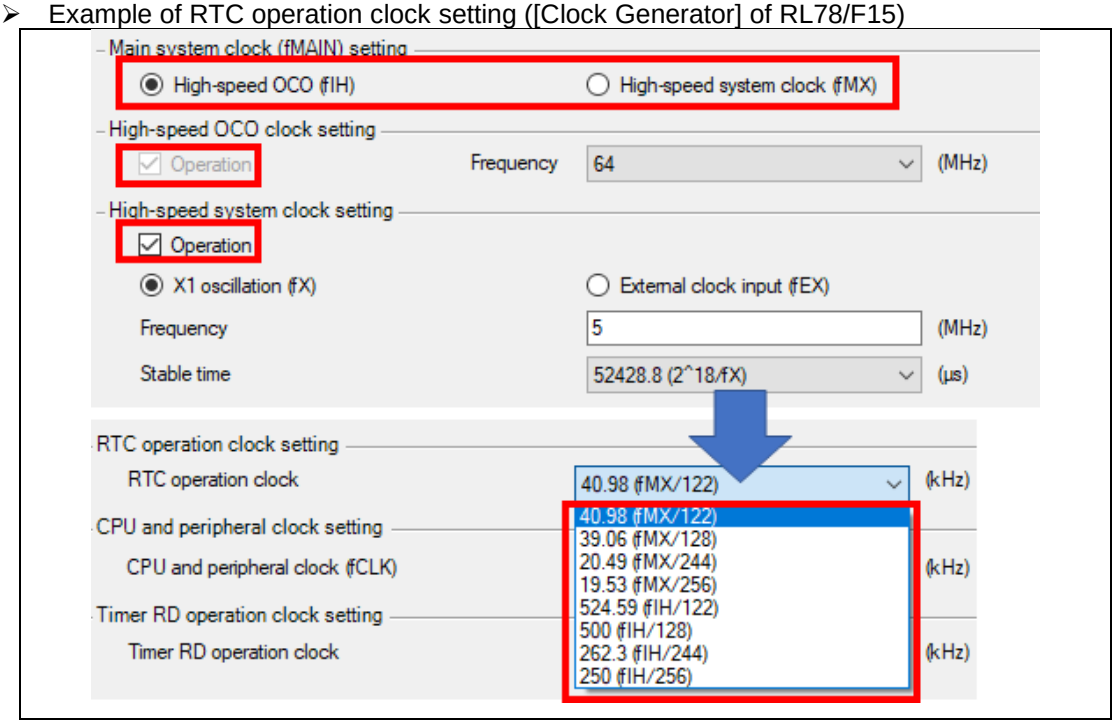
2.2 Applicable Devices

RL78 family: RL78/F13, RL78/F14, RL78/F15, and RL78/D1A group

2.3 Details

When you select fMX or fIH divided clock in the [RTC operation clock setting] of the [Clock Generator] of the applicable products, incorrect code is generated. Because the procedure for setting the RTCC register differs from the one in the User's Manual for the applicable devices, RTC operation might be affected.

- Example of RTC operation clock setting ([Clock Generator] of RL78/F15)



Note: The options in [RTC operation clock setting] vary depending on the [Main system clock (fMAIN) setting] and whether the [Operation] checkbox is checked in the [High-speed OCO clock setting] and [High-speed system clock setting].

2.4 Workaround

After generating code, open R_CGC_Create(void) in the r_cg_cgc.c. Set the RTCCL_7(Note1) bit in the RTC clock select register (RTCCL), as written in the User's Manual for the applicable devices, and then set the RTCCKS1, RTCCKS0 and RTCCL_6 (Note2) bits.

Note 1: RTCCL7 for the RL78/D1A group

Note 2: RTCCL6 for the RL78/D1A group

The setting example is shown below. Modify the code in the red box and blue box (Note).

Note that if you perform code generation again, the modified code (above) will be overwritten. Thus, you will need to modify the code in the steps above after each code generation.

Note: The code in the red box and blue box varies depending on which item is selected in the [RTC operation clock setting]. For details, refer to the User's Manual for the applicable devices.

➢When fMX divided clock is selected in [RTC operation clock setting]

Before modification

```
void R_CGC_Create(void)
{
    /* Set fIH */
    HIOSTOP = 0U;
    /* Set RTC clock source */
    RTCCL = _00_CGC_RTC_FMX | _42_CGC_RTC_DIV122;
    /* Set Timer RD clock source to fCLK, fMP */
    TRD_CKSEL = 0U;
}
```

After modification

```
void R_CGC_Create(void)
{
    /* Set RTC clock source */
    RTCCL = _00_CGC_RTC_FMX;

    RTCCL |= _42_CGC_RTC_DIV122;
    /* Set Timer RD clock source to fCLK, fMP */
    TRD_CKSEL = 0U;
}
```

- When fIH divided clock is selected in [RTC operation clock setting]

Before modification

```
void R_CGC_Create(void)
{
    /* Set RTC clock source */
    RTCCL = _80_CGC_RTC_FIH | _42_CGC_RTC_DIV122;
    /* Set Timer RD clock source to fCLK, fMP */
    TRD_CKSEL = 0U;
}
```

After modification

```
void R_CGC_Create(void)
{
    /* Set RTC clock source */
    RTCCL = _80_CGC_RTC_FIH;
    RTCCL |= _42_CGC_RTC_DIV122;
    /* Set Timer RD clock source to fCLK, fMP */
    TRD_CKSEL = 0U;
}
```

2.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in July 2019.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun.01.19	-	First edition issued

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