RENESAS Tool News

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A Note on Using the Simulator Debugger--R32C V.1.00 Release 00-- for the R32C/100 MCU series

Please take note of the following problem in using the simulator debugger --R32C V.1.00 Release 00--for the R32C/100 MCU series:

- With using Bank1 register direct of Extended Instruction Addressing

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1. Description

If you perform an operation by applying Bank1 register direct of Extended Instruction Addressing to the dest operand of a multiplication or division instruction with the B flag of the FLG register cleared to "0", the B flag may be set to "1".

1.1 Conditions

This problem occurs if either of the following conditions is satisfied:

(1) In the EMUL and EMULU instructions, Bank1 register direct is applied to the dest operand.

(2) In the EDIV, EDIVU, and EDIVX instructions, either of the following conditions is met:

(a) ".B" is used as the size specifier (.size), the divisor (the src operand) is not "0", and the dest operand is stored in the R2B register.

(b) ".W" is used as the size specifier (.size), the divisor (the src operand) is not "0", and the dest operand is stored in the R3R1B register.

NOTICE:

The above-formatted instructions are not generated by the C compiler for the R32C/100 MCU series; this problem concerns with

debugging the programs generated by assemblers.

2. Workaround

After executing each of the instructions concerned, clear the B flag to "0".

Example:

```
EMUL.B R1L, R0LB  ;  Instruction concerned
FCLR B            ;  B flag cleared
```

3. Schedule of Fixing the Problem

We plan to fix this problem in the next release of the product.
