RENESAS Tool News

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Note on Using RX210 Group Renesas Peripheral Driver Library and Peripheral Driver Generator

When using RX210 Group Renesas Peripheral Driver Library and Peripheral Driver Generator, take note of the following problem:

- With setting the system clock

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1. Products and Versions Concerned

- RX210 Group Renesas Peripheral Driver Library Rev.1.01
- Peripheral Driver Generator V.2.03 through V.2.06

2. Description

If you pass values within a specified range as arguments to the R_CGC_Set or R_CGC_Control function, the MOFCR.MODRV2[2:0] bit, which selects an oscillation drivability of the main clock, is set to an incorrect value.

3. Conditions

3.1 In RX210 Group Renesas Peripheral Driver Library

The problem arises if either of the following conditions is satisfied:

(1) In the R_CGC_Set function, value "PDL_CGC_CLK_MAIN" is passed as the first argument, and a value equal to or greater than 1 MHz and less than 16 MHz is passed as the third argument.

(2) In the R_CGC_Control function, value "PDL_CGC_MAIN_1_8" or "PDL_CGC_MAIN_8_16" is passed as the second argument.

3.2 IN Peripheral Driver Generator

This problem arises if the following conditions are all satisfied:

(1) The main clock oscillator is used in the clock generation circuit of any MCU of the RX210 group.

(2) A crystal resonator is selected from the main clock oscillation source pull-down menu of the clock generation circuit.

(3) A value less than 16 MHz is typed into the main clock (EXTAL input)

frequency text box of the clock generation circuit.

4. Workarounds

4.1 In RX210 Group Renesas Peripheral Driver Library

(1) In the R_CGC_Set function, after making a call to the R_CGC_Set function concerned, set the MOFCR.MODRV2[2:0] bit to the correct value.

Example:

```
-------------------------------------------------
res = R_CGC_Set(
   PDL_CGC_CLK_MAIN,
   PDL_CGC_BCLK_DISABLE | PDL_CGC_MAIN_RESONATOR,
   8E6,
   8E6,
   8E6,
   8E6,
   8E6,
   8E6
);

 /* Workaround started */
SYSTEM.PRCR.WORD = 0xA507;
        /* Protection of SYSTEM-related registers disabled */
SYSTEM.MOFCR.BIT.MODRV2 = 1;
        /* Drivability of main clock oscillator is set to "01b"
           for frequency range of 1 MHz to 8 MHz, or to "10b"
           for frequency range of 8.1 MHz to 15.9 MHz */
SYSTEM.PRCR.WORD = 0xA500;
        /* Protection of SYSTEM-related registers enabled */
/* Workaround ended */
-------------------------------------------------
```

(2) In the R_CGC_Control function, pass neither "PDL_CGC_MAIN_1_8" nor "PDL_CGC_MAIN_8_16" as the second arguments to the function. If you make a change to the drivability, set the MOFCR.MODRV2 bit directly.

4.2 In Peripheral Driver Generator

Within the R_PG_Clock_Set function generated by Peripheral Driver Generator, place the code for setting the MOFCR.MODRV2[2:0] bit before the code for making a call to the R_CGC_Control function.

Or if you use the R_PG_Clock_WaitSet function, place the code for setting the MOFCR.MODRV2[2:0] bit before the code for making a call

to the rpdl_wait_time function.

Example:

```
-------------------------------------------------
bool R_PG_Clock_WaitSet(double wait_time)
{
   bool res;

   res = R_CGC_Set(
      PDL_CGC_CLK_LOCO,
      PDL_CGC_BCLK_DISABLE,
      125000,
      125000.000000,
      125000.000000,
      125000.000000,
      125000.000000,
      125000.000000
   );

   if( !res ){
      return res;
   }

   /* Call to function concerned */
   res = R_CGC_Set(
      PDL_CGC_CLK_MAIN,
      PDL_CGC_BCLK_DISABLE | PDL_CGC_MAIN_RESONATOR,
      10000000,
      10000000.000000,
      10000000.000000,
      10000000.000000,
      10000000.000000,
      10000000.000000
   );

   if( !res ){
      return res;
   }

   res = R_CGC_Set(
      PDL_CGC_CLK_PLL,
      PDL_CGC_BCLK_DISABLE,
      100000000,
      50000000.000000,
      25000000.000000,
```

```
    25000000.000000,
    25000000.000000,
    25000000.000000
  );

  if( !res ){
    return res;
  }

  /* Workaround started */
  SYSTEM.PRCR.WORD = 0xA507;
        /* Protection of SYSTEM-related registers disabled */

  SYSTEM.MOFCR.BIT.MODRV2 = 2;
        /* Drivability of main clock oscillator is set to "10b"
           for frequency range of 8.1 MHz to 15.9 MHz, or to
           "01b" for frequency range of 1 MHz to 8 MHz */
  SYSTEM.PRCR.WORD = 0xA500;
        /* Protection of SYSTEM-related registers enabled */
  /* Workaround ended */

  rpdl_wait_time( wait_time );

  return R_CGC_Control(
    PDL_CGC_CLK_PLL,
    PDL_CGC_OSC_STOP_DISABLE,
    PDL_NO_DATA
  );
}
-------------------------------------------------
```

5. Schedule of Fixing Problem

We plan to fix this problem in a future release of each product.
