RENESAS Tool News

RENESAS TOOL NEWS on September 1, 2013: 130901/tn3

Note on Using Renesas Peripheral Driver Libraries for RX630/RX63N/RX631/RX210 Groups of MCUs and Peripheral Driver Generator -- With Using an External Clock in the 16-bit Timer Pulse Unit (TPUa) --

When using Renesas Peripheral Driver Libraries for the RX630/RX63N/RX631/ RX210 groups of MCUs and Peripheral Driver Generator, take note of the following problem:

- With using an external clock in the 16-bit timer pulse unit (TPUa)

---

1. Products and Versions Concerned

- RX630 Group Renesas Peripheral Driver Library V.1.00 or later
- RX63N, RX631 Group Renesas Peripheral Driver Library V.1.01 or later
- RX210 Group Renesas Peripheral Driver Library V.2.00 or later
- Peripheral Driver Generator V.2.03 or later

2. Description

When an external clock is used for a counter clock of TPUa (including the case when the phase-counting mode is in use), the external clock input pins (TCLKn; n: A to H) may not be correctly set.

3. Condition

This problem may arise if multiple channels are used in the same unit (see NOTE) and an external clock is used in any of those channels, except when all channels used in the same unit use the same external clocks.

NOTE:
Two units (six channels for each unit) are incorporated in RX630, RX63N, and RX631 groups and one unit (six channels) is incorporated in RX210 group.
The target modules are as follows:

- TPU unit 0: TPU0 to TPU5
- TPU unit 1: TPU6 to TPU11

4. Examples

4.1 In Renesas Peripheral Driver Library

The external clock input pins that have been set first by using the R_TPU_Set function are disabled by the R_TPU_Set function to be called later. (see NOTE)

NOTE:
The pin function control register (PmnPFS) is cleared to 0.

Example:
When TCLKC and TCLKD are used in TPU2 and TCLKA and TCLKB are used in TPU5

```
-----------------------------------------------------------------------
R_TPU_Set(
   2,
   PDL_TPU_PIN_CLKC_P16 | PDL_TPU_PIN_CLKD_P17
);
//TCLKC and TCLKD are set.

R_TPU_Set(
   5,
   PDL_TPU_PIN_CLKA_P14 | PDL_TPU_PIN_CLKB_P15
);
//TCLKA and TCLKB are set. TCLKC and TCLKD that have been set first
  are disabled.
-----------------------------------------------------------------------
```

4.2 In Peripheral Driver Generator

The external clock input pins used on the channel set first by using the R_PG_TimerStart_TPU_Um_Cn function are disabled by the R_PG_TimerStart_TPU_Um_Cn function to be called later. (see NOTE)

NOTE:
The pin function control register (PmnPFS) and the port mode register (PMR) are cleared to 0.

Example:
When TPU2 is set for the phase-counting mode (using TCLKC and TCLKD) and TPU5 is set for the phase-counting mode (using TCLKA and TCLKB)

```
-----------------------------------------------------------------------
R_PG_TimerStart_TPU_U0_C2();  //TCLKC and TCLKD are set.
R_PG_TimerStart_TPU_U0_C5();  //TCLKA and TCLKB are set. TCLKC and TCLKD
```

that have been set first are disabled.

---

5. Workaround

5.1 In Renesas Peripheral Driver Library

In the R_TPU_Set function to be called later, set all external clock input pins used by channels in the same unit.

Example:
When TCLKC and TCLKD are used in TPU2 and TCLKA and TCLKB are used in TPU5

```
R_TPU_Set(
   2,
   PDL_TPU_PIN_CLKC_P16 | PDL_TPU_PIN_CLKD_P17
);

R_TPU_Set(
   5,
   PDL_TPU_PIN_CLKA_P14 | PDL_TPU_PIN_CLKB_P15 |
   PDL_TPU_PIN_CLKC_P16 | PDL_TPU_PIN_CLKD_P17  /* Workaround: Set the
                                external clock input
                                pins that have been
                                set first. */
);
```

5.2 In Peripheral Driver Generator

To reset the disabled external clock input pins, directly set the pin function control register (PmnPFS) and the port mode register (PMR).

Example:
When TPU2 is set for the phase-counting mode (using TCLKC and TCLKD) and TPU5 is set for the phase-counting mode (using TCLKA and TCLKB)

```
R_PG_TimerStart_TPU_U0_C2();
R_PG_TimerStart_TPU_U0_C5();

/* Here begins workaround */
//Set PmnPFS and PMR to enable TCLKC and TCLKD.
//Disable register write protection.
MPC.PWPR.BIT.B0WI = 0;
MPC.PWPR.BIT.PFSWE = 1;

//Set PmnPFS.
```

```
MPC.P16PFS.BIT.PSEL = 0x4; //P16: TCLKC
MPC.P17PFS.BIT.PSEL = 0x4; //P17: TCLKD

//Enable register write protection.
MPC.PWPR.BYTE = BIT_7;

//Set PMR.
PORT1.PMR.BIT.B6 = 1; //P16: peripheral functions selected
PORT1.PMR.BIT.B7 = 1; //P17: peripheral functions selected
/* Here ends workaround */
```
---

6. Schedule for Fixing the Problem

This problem will be fixed at a later revision of the product.
