RENESAS Tool News

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Note on Using Peripheral Driver Generator V.2.03

When using Peripheral Driver Generator V.2.03, take note of the following problem:

- With setting the clock generator circuit on an MCU of the RX210 group

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1. Description

To make the initial setting of the clock generator circuit on an MCU of the RX210 group, you can use the R_PG_Clock_Set function generated by Peripheral Driver Generator V.2.03. If you make a call to this function within the user program, it may return a value of "false", and you cannot set up the clock generator.

2. Conditions

This problem arises in the MCUs of the RX210 series if the inputs to the window for setting clock generation circuit (the SYSTEM tab) satisfy any of the following conditions.

(1) Any of the following internal-clock-frequency division ratios, which are displayed in the Frequency Settings area, is greater than 16:

- Internal clock source frequency division ratio of System Clock (ICLK)
- Internal clock source frequency division ratio of Peripheral Module Clock B (PCLKB)
- Internal clock source frequency division ratio of Peripheral Module Clock D (PCLKD)
- Internal clock source frequency division ratio of FlashIF Clock (FCLK)
- Internal clock source frequency division ratio of External Bus Clock (BCLK)

(2) If the value displayed in the Internal Clock Source Frequency text box is divided by any of the following actual values, the quotient is not an integer for all the divisions:
- Actual value of System Clock (ICLK)
- Actual value of Peripheral Modules Clock B (PCLKB)
- Actual value of Peripheral Module Clock D (PCLKD)
- Actual value of FlashIF Clock (FCLK)
- Actual value of External Bus Clock (BCLK)

(3) Suppose that from among the Internal Clock Source drop-down list box, you have selected any one except Main Clock and PLL Circuit, and then selected the Use the Main Clock Oscillator check box. If the value in the Main Clock (EXTAL Input) Frequency text box expressed in Hz is divided by any of the following internal-clock-frequency ratios, the quotient is not an integer for all the divisions:
- Internal clock source frequency division ratio of System Clock (ICLK)
- Internal clock source frequency division ratio of Peripheral Module Clock B (PCLKB)
- Internal clock source frequency division ratio of Peripheral Module Clock D (PCLKD)
- Internal clock source frequency division ratio of FlashIF Clock (FCLK)
- Internal clock source frequency division ratio of External Bus Clock (BCLK)

3. Workaround

If the problem arises, do not use the R_PG_Clock_Set function to make the initial setting of the clock generator circuit.

4. Schedule of Fixing Problem

We plan to fix this problem in Peripheral Driver Generator V.2.04.