

Note on Using Code Generator for RX Family Managed by CS+

When using CS+ Code_Generator for RX, the code generator for the RX Family managed by CS+, take note of the problems on the following points that are described in this note:

1. Settings for clocks in the output code
(applicable products: RX64M group)
 2. Bus settings
(applicable products: RX64M group)
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1. Settings for Clocks in the Output Code (Applicable Products: RX64M Group)

1.1 Product and Version Concerned

CS+ Code_Generator for RX V1.04.00

1.2 MCUs Concerned

RX Family: RX64M group

1.3 Description

There is an error in the output code of the void R_CGC_Create(void) function, which is in the r_cg_cgc.c source file for clock settings.

In writing a value to system clock control register 2 (SCKCR2), bit 0 is erroneously set to "0". The correct setting for bit 0 is "1".

1.4 Workaround

Modify the setting for SCKCR2 in void R_CGC_Create(void).

Before modification:

```
-----  
/* Set UCLK */  
SYSTEM.SCKCR2.WORD = xxxx;  
-----
```

After modification:

```
-----  
/* Set UCLK */  
SYSTEM.SCKCR2.WORD = xxxx + 1; <- Set bit 0 of register SCKCR2 to "1".  
-----
```

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version.

2. Bus Settings (Applicable Products: RX64M Group)

2.1 Product and Version Concerned

CS+ Code_Generator for RX V1.04.00

2.2 MCUs Concerned

RX Family: RX64M group

2.3 Description

When setting a separate bus in the interface for bus area settings, the address latch signal (ALE) has to be enabled.

The use of a separate bus was originally selectable regardless of the ALE setting.

2.4 Workaround

Enable ALE.

If the ALE setting creates a problem, modify the source code which resets the ALE setting after code generation.

2.5 Schedule for Fixing the Problem

This problem will be fixed in the next version.

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