RENESAS Tool News

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Note on Using Code Generator for RL78 Family Managed by CS+ (CS+ for CA, CX)

When using "CS+ for CA, CX Code_Generator for RL78", the code generator for the RL78 family managed by CS+, take note of the problems on the following points that are described in this note.

1. Code Generated for Comparator Settings
   (Applicable Products: RL78/I1A Group)

2. DTC Settings
   (Applicable Products: RL78/F13, RL78/F14 Groups)

3. Setting the Voltage Detection Circuit to "Interrupt Mode"
   (Applicable Products: RL78/L12, RL78/I1A, RL78/G1A, RL78/F13, and RL78/F14 Groups)

4. Saving Projects with Settings for the A/D Convertor
   (Applicable Products: RL78/L1C Group)

5. Reflection of Pin Configurations in Generated Code
   (Applicable Products: RL78/G12, RL78/G13, and RL78/G14 Groups)

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1. Code Generated for Comparator Settings

1.1 Product and Version Concerned

CS+ for CA, CX Code_Generator for RL78 V2.05.00

1.2 MCUs Concerned

RL78 Family: RL78/I1A group MCUs in 30-pin packages

1.3 Description

When a comparator is set, code for clock supply is not output.

1.4 Workaround

Add the statement for clock supply given below at the beginning of the

comparator initialization function (R_COMP_Create() in r_cg_comp.c) after the code has been generated.

```
PGACMPEN = 1U;  /* Supply the comparator clock. */
```

This should be added every time code is generated.

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version.

2. DTC Settings

2.1 Product and Version Concerned

CS+ for CA, CX Code_Generator for RL78 V2.05.00

2.2 MCUs Concerned

RL78 Family: RL78/F13, RL78/F14 groups

2.3 Description

(1) A project is not saved after code generation when high-speed transfer by the DTC is set.

(2) DTC activating source numbers are not set correctly for the DTC vector addresses.

2.4 Workaround

(1) For 2.3 (1)

After generating code, release the setting for high-speed transfer by the DTC before saving the project.

(2) For 2.3 (2)

After generating code, make correct DTC vector address settings (*) in the DTC initialization function (void R_DTC_Create() in r_cg_dtc.c) with reference to the manual indicated below.

Note that the above modification will be needed every time code is generated.

*: x in dtc_vectortable[x] is the number of the activating source.

RL78/F13, F14 User's Manual: Hardware

Table 19-5 DTC Activation Sources and DTC Vector Addresses

https://www.renesas.com/search/keyword-search.html#genre=document&q=r01uh0368

Example of the modification: Setting the completion of reception by UART0 as the source for DTC activation

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Set the correct activating source number "10" (reception by

UART0 completed, transfer by CSI01 completed or CSI01 buffer is empty, or transfer by IIC01 completed), otherwise the wrong activating source number "9" (A/D conversion completed) will be set.

Before modification: dtc_vectortable[9] = xx;
After modification: dtc_vectortable[10] = xx;
xx: Output value of code generation

2.5 Schedule for Fixing the Problem

This problem will be fixed in the next version.

3. Setting the Voltage Detection Circuit to "Interrupt Mode"

3.1 Product and Version Concerned

CS+ for CA, CX Code_Generator for RL78 V2.05.00

3.2 MCUs Concerned

RL78 Family: RL78/L12, RL78/I1A, RL78/G1A, RL78/F13, and RL78/F14 groups

3.3 Description

Operation of the voltage detection circuit is in "reset mode" even if "interrupt mode" is selected.

3.4 Workaround

Modify bit 1 of the following value to "0" after code generation.

Value to be modified: 000C1H/010C1H of "User option byte value" which is in the Link Options tabbed page of CA78K0R (build tool)

Note that the above modification will be needed every time code is generated.

Modification example: Setting the RL78/F13 voltage detection circuit to interrupt mode with interrupt generation at the voltage 2.75 V.

Modify the value for "User option byte value" at 000C1H/010C1h to 7D from 7F.

Before modification: xx7Fyy
After modification: xx7Dyy
xx: Setting of 000C0H/010C0H; yy: setting of 000C2H/010C2H

3.5 Schedule for Fixing the Problem
This problem will be fixed in the next version.

4. Saving Projects with Settings for the A/D Convertor
4.1 Product and Version Concerned
CS+ for CA, CX Code_Generator for RL78 V2.05.00

4.2 MCUs Concerned
RL78 Family: RL78/L1C group

4.3 Description
When a project configured with the below settings for the A/D convertor is read, the "A fatal error occurred" dialog box is displayed, after which CS+ operation is terminated.
- Selection of analog input pins from among ANI0-ANI2, ANI5, and ANI6:
  ANI0-ANI1
- VREF(+) setting:
  AVREFP
- VREF(-) setting:
  AVREFM

4.4 Workaround
After the code generation, change the setting for "analog input pin setting for ANI0-ANI2, ANI5, and ANI6" to "ANI0-ANI2" and save the project.

4.5 Schedule for Fixing the Problem
This problem will be fixed in the next version.

5. Reflection of Pin Configurations in Generated Code
5.1 Product and Version Concerned
CS+ for CA, CX Code_Generator for RL78 V2.05.00

5.2 MCUs Concerned
RL78 Family: RL78/G12, RL78/G13, and RL78/G14 groups

5.3 Description
When the "Reflect PIN" button is pressed after setting the input/output modes of port pins, "I/O" is always displayed regardless of the selected input/output modes.

5.4 Workaround

There is no way to prevent this problem.
Note that you can still use the C source code since the problem does not affect the generated C source code.

5.5 Schedule for Fixing the Problem

This problem will be fixed in the next version.
