

Customer Notification

V850E/Sx3-H

32-Bit Single-Chip Microcontroller

Operating Precautions

V850E/SJ3-H:

μPD70F3474
μPD70F3474A
μPD70F3475
μPD70F3475A
μPD70F3476
μPD70F3476A
μPD70F3477
μPD70F3477A
μPD70F3478
μPD70F3478A
μPD70F3479
μPD70F3479A
μPD70F3931
μPD70F3931A
μPD70F3932
μPD70F3932A

μPD70F3933
μPD70F3933A
μPD70F3934
μPD70F3934A
μPD70F3935
μPD70F3935A
μPD70F3936
μPD70F3936A
μPD70F3937
μPD70F3937A
μPD70F3938
μPD70F3938A
μPD70F3939
μPD70F3939A

V850E/SK3-H:

μPD70F3480
μPD70F3480A
μPD70F3481
μPD70F3481A
μPD70F3482
μPD70F3482A
μPD70F3486
μPD70F3486A
μPD70F3487
μPD70F3487A
μPD70F3488
μPD70F3488A
μPD70F3925
μPD70F3925A
μPD70F3926
μPD70F3926A

μPD70F3927
μPD70F3927A

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Operating Precautions for V850E/Sx3-H

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(A) Table of Operating Precautions

V850E/SJ3-H

Outline		μPD70F3474 μPD70F3475 μPD70F3476 μPD70F3477 μPD70F3478 μPD70F3479 μPD70F3931 μPD70F3932 μPD70F3933 μPD70F3934 μPD70F3935 μPD70F3936 μPD70F3937 μPD70F3938 μPD70F3939			μPD70F3474A μPD70F3475A μPD70F3476A μPD70F3477A μPD70F3478A μPD70F3479A μPD70F3931A μPD70F3932A μPD70F3933A μPD70F3934A μPD70F3935A μPD70F3936A μPD70F3937A μPD70F3938A μPD70F3939A		
	Rev.	V1.0	V1.1	V1.2	V1.3		
	Rank ^a	I	I	I	I		
No. 1	External memory bus interface in 8-bit multiplexed mode (Technical Limitation)	x	x	✓	✓		
No. 2	Connection of HLDK signal to Port CT (Specification Change Notice)	x	x	x	✓		

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

✓: Not applicable

x: Applicable

V850E/SK3-H

Outline		μPD70F3480 μPD70F3481 μPD70F3482 μPD70F3486 μPD70F3487 μPD70F3488 μPD70F3925 μPD70F3926 μPD70F3927			μPD70F3480A μPD70F3481A μPD70F3482A μPD70F3486A μPD70F3487A μPD70F3488A μPD70F3925A μPD70F3926A μPD70F3927A	
	Rev.	V1.0	V1.1	V1.2	V1.3	
	Rank ^a	I	I	I	I	
No. 1	External memory bus interface in 8-bit multiplexed mode (Technical Limitation)	x	x	✓	✓	
No. 2	Connection of HLDK signal to Port CT (Specification Change Notice)	x	x	x	✓	

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

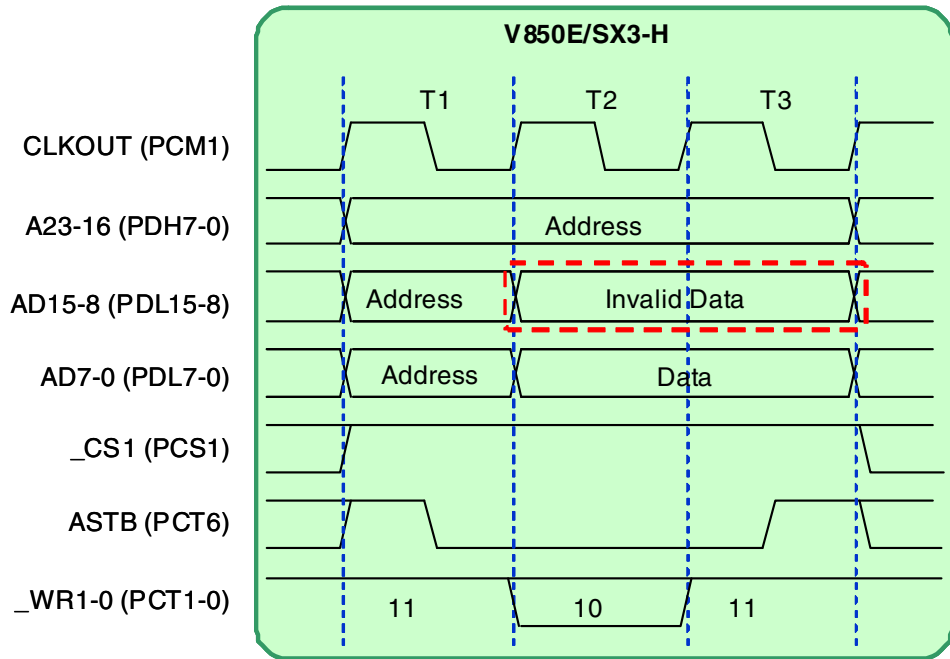
✓: Not applicable
 x: Applicable

(B) Description of Operating Precautions

No. 1 External memory bus interface in 8-bit multiplexed mode (Technical Limitation)

Details:

When using the external memory bus interface in 8-bit multiplexed mode invalid data is output on the AD15...AD8 pins. The AD15...AD8 pins do not keep the output address signals in T2 and T3 states of the external memory bus cycle (“Invalid Data”).



Workaround:

An external latch can be used to latch the address information on AD15...AD8 during T1 phase of the bus cycle (same as AD7...AD0).

This behaviour will be changed in Version 1.2 of the device.

No. 2 Connection of HLDK signal to Port CT (Specification Change Notice)

Details:

If the bus hold function is used to grant control of the external memory bus to an external bus master the bus control lines of Port CT (WR0, WR1, RD, ASTB) do not become Hi-Z. Instead they output logical high level.

Therefore the bus hold function does not operate as expected.

The bus hold function is used in multi processor systems or multi bus master systems.

The behaviour does not occur if the bus hold function is not used.

Other ports of the external memory bus are not concerned.

Workaround:

There is no workaround. Do not use the bus hold function.

(C) Valid Specification

Item	Date published	Document No.	Comment
1	May 2009	U19201EJ2V0UD00	V850E/Sx3-H Hardware (User's Manual)

(D) Revision History

Item	Date published	Document No.	Comment
1	March 2009	U19703EE1V0IF00	Initial release.
2	May 2009	U19703EE1V11F00	Added device versions ES1.1 and CS 1.2, modified item 1, modified table of operating precautions.
3	November 2009	U19703EE2V0IF00	Added item 2.

