

RENESAS TECHNICAL UPDATE

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 Renesas Electronics Corporation

Product Category	MPU/MCU	Document No.	TN-V85-A022A/E	Rev.	1.00
Title	V850E/SV2 Usage Restriction about bus control function.		Information Category	Usage Restriction	
Applicable Product	V850E/SV2 series	Lot No.	Reference Document	* Preliminary User's Manual V850EV2 32-Bit Single-Chip Microcontroller Hardware v1.00 (the 1st edition) U16384JJ1V1UD00	
		All lots			

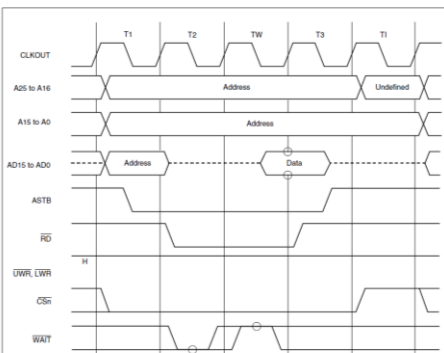
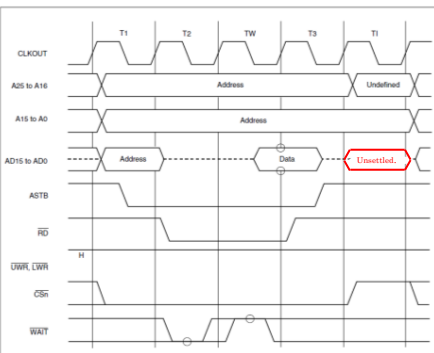
A restriction matter of a bus control function was revealed about V850E/SV2.

1. Detail of restriction

When using a bus control function, AD0-AD15 terminal becomes unsettled at idle State.

User's manual are corrected as follows.

Item	Page	Correction point	Current state.	After restriction																																																																																																																																																												
1.	53	2.2 Pin status (Table)	<table border="1"> <thead> <tr> <th>Operating Status</th> <th>Reset***</th> <th>HALT Mode/ During DMA Transfer</th> <th>IDLE Mode/ Software STOP Mode</th> <th>Idle State</th> <th>Bus Hold</th> </tr> </thead> <tbody> <tr> <td>Pin</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>AD0 to AD15 (PDL0 to PDL15)</td> <td>Hi-Z</td> <td>Operating</td> <td>Hi-Z</td> <td>Hold</td> <td>Hi-Z</td> </tr> <tr> <td>A0 to A15*** (P90 to P915)</td> <td>Hi-Z</td> <td>Operating</td> <td>Hi-Z</td> <td>Hold</td> <td>Hi-Z</td> </tr> <tr> <td>A16 to A25 (PDH0 to PDH9)</td> <td>Hi-Z</td> <td>Operating</td> <td>Hi-Z</td> <td>Hold</td> <td>Hi-Z</td> </tr> <tr> <td>CS0 to CS7 (PCS0 to PCS7)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>Hold</td> <td>Hi-Z</td> </tr> <tr> <td>LWR, UWR (PCT0, PCT1)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>Hi-Z</td> </tr> <tr> <td>RD (PCT4)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>Hi-Z</td> </tr> <tr> <td>ASTB (PCT6)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>Hi-Z</td> </tr> <tr> <td>WAIT (PCM0)</td> <td>Hi-Z</td> <td>Operating</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>CLKOUT (PCM1)</td> <td>Hi-Z</td> <td>Operating</td> <td>L</td> <td>Operating</td> <td>Operating</td> </tr> <tr> <td>HLDAR (PCM2)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>HLDRO (PCM3)</td> <td>Hi-Z</td> <td>Operating</td> <td>-</td> <td>-</td> <td>Operating</td> </tr> </tbody> </table>	Operating Status	Reset***	HALT Mode/ During DMA Transfer	IDLE Mode/ Software STOP Mode	Idle State	Bus Hold	Pin						AD0 to AD15 (PDL0 to PDL15)	Hi-Z	Operating	Hi-Z	Hold	Hi-Z	A0 to A15*** (P90 to P915)	Hi-Z	Operating	Hi-Z	Hold	Hi-Z	A16 to A25 (PDH0 to PDH9)	Hi-Z	Operating	Hi-Z	Hold	Hi-Z	CS0 to CS7 (PCS0 to PCS7)	Hi-Z	Operating	H	Hold	Hi-Z	LWR, UWR (PCT0, PCT1)	Hi-Z	Operating	H	H	Hi-Z	RD (PCT4)	Hi-Z	Operating	H	H	Hi-Z	ASTB (PCT6)	Hi-Z	Operating	H	H	Hi-Z	WAIT (PCM0)	Hi-Z	Operating	-	-	-	CLKOUT (PCM1)	Hi-Z	Operating	L	Operating	Operating	HLDAR (PCM2)	Hi-Z	Operating	H	H	L	HLDRO (PCM3)	Hi-Z	Operating	-	-	Operating	<table border="1"> <thead> <tr> <th>Operating Status</th> <th>Reset***</th> <th>HALT Mode/ During DMA Transfer</th> <th>IDLE Mode/ Software STOP Mode</th> <th>Idle State</th> <th>Bus Hold</th> </tr> </thead> <tbody> <tr> <td>Pin</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>AD0 to AD15 (PDL0 to PDL15)</td> <td>Hi-Z</td> <td>Operating</td> <td>Hi-Z</td> <td>Hi-Z</td> <td>Hi-Z</td> </tr> <tr> <td>A0 to A15*** (P90 to P915)</td> <td>Hi-Z</td> <td>Operating</td> <td>Hi-Z</td> <td>Hold</td> <td>Hi-Z</td> </tr> <tr> <td>A16 to A25 (PDH0 to PDH9)</td> <td>Hi-Z</td> <td>Operating</td> <td>Hi-Z</td> <td>Hold</td> <td>Hi-Z</td> </tr> <tr> <td>CS0 to CS7 (PCS0 to PCS7)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>Hold</td> <td>Hi-Z</td> </tr> <tr> <td>LWR, UWR (PCT0, PCT1)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>Hi-Z</td> </tr> <tr> <td>RD (PCT4)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>Hi-Z</td> </tr> <tr> <td>ASTB (PCT6)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>Hi-Z</td> </tr> <tr> <td>WAIT (PCM0)</td> <td>Hi-Z</td> <td>Operating</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>CLKOUT (PCM1)</td> <td>Hi-Z</td> <td>Operating</td> <td>L</td> <td>Operating</td> <td>Operating</td> </tr> <tr> <td>HLDAR (PCM2)</td> <td>Hi-Z</td> <td>Operating</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>HLDRO (PCM3)</td> <td>Hi-Z</td> <td>Operating</td> <td>-</td> <td>-</td> <td>Operating</td> </tr> </tbody> </table>	Operating Status	Reset***	HALT Mode/ During DMA Transfer	IDLE Mode/ Software STOP Mode	Idle State	Bus Hold	Pin						AD0 to AD15 (PDL0 to PDL15)	Hi-Z	Operating	Hi-Z	Hi-Z	Hi-Z	A0 to A15*** (P90 to P915)	Hi-Z	Operating	Hi-Z	Hold	Hi-Z	A16 to A25 (PDH0 to PDH9)	Hi-Z	Operating	Hi-Z	Hold	Hi-Z	CS0 to CS7 (PCS0 to PCS7)	Hi-Z	Operating	H	Hold	Hi-Z	LWR, UWR (PCT0, PCT1)	Hi-Z	Operating	H	H	Hi-Z	RD (PCT4)	Hi-Z	Operating	H	H	Hi-Z	ASTB (PCT6)	Hi-Z	Operating	H	H	Hi-Z	WAIT (PCM0)	Hi-Z	Operating	-	-	-	CLKOUT (PCM1)	Hi-Z	Operating	L	Operating	Operating	HLDAR (PCM2)	Hi-Z	Operating	H	H	L	HLDRO (PCM3)	Hi-Z	Operating	-	-	Operating
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3.	142	Fig 4-5. With Idle State Inserted	<p>Notes 1. AD0 to AD7 retain the address output at that time when an odd address is accessed for byte data. AD8 to AD15 retain the address output at that time when an even address is accessed for byte data.</p> <p>2. CSn (n = 7 to 0) goes low as shown above if the corresponding CSn area is accessed. Otherwise, CSn will remain high.</p> <p>Remarks 1. The circles indicate the sampling timing.</p> <p>2. The broken lines indicate the high-impedance state.</p>	<p>Notes 1. AD0 to AD7 retain the address output at that time when an odd address is accessed for byte data. AD8 to AD15 retain the address output at that time when an even address is accessed for byte data.</p> <p>2. CSn (n = 7 to 0) goes low as shown above if the corresponding CSn area is accessed. Otherwise, CSn will remain high.</p> <p>Remarks 1. The circles indicate the sampling timing.</p> <p>2. The broken lines indicate the high-impedance state.</p>																																																																																																																																																												

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4.	143	Fig 4-5. With Wait State (1 Wait) and Idle State Inserted	<p style="text-align: center;">Figure 4-6. With Wait State (1 Wait) and Idle State Inserted</p>  <p>Notes</p> <ol style="list-style-type: none"> 1. AD0 to AD7 retain the address output at that time when an odd address is accessed for byte data. AD8 to AD15 retain the address output at that time when an even address is accessed for byte data. 2. CSn (n = 7 to 0) goes low as shown above if the corresponding CSn area is accessed. Otherwise, CSn will remain high. <p>Remarks</p> <ol style="list-style-type: none"> 1. The circles indicate the sampling timing. 2. The broken lines indicate the high-impedance state. 	<p style="text-align: center;">Figure 4-6. With Wait State (1 Wait) and Idle State Inserted</p>  <p>Notes</p> <ol style="list-style-type: none"> 1. AD0 to AD7 retain the address output at that time when an odd address is accessed for byte data. AD8 to AD15 retain the address output at that time when an even address is accessed for byte data. 2. CSn (n = 7 to 0) goes low as shown above if the corresponding CSn area is accessed. Otherwise, CSn will remain high. <p>Remarks</p> <ol style="list-style-type: none"> 1. The circles indicate the sampling timing. 2. The broken lines indicate the high-impedance state.

2. Workaround

When using the bus function, be careful so that a signal of AD0-AD15 terminal doesn't collide with idle state.

This issue is not planned for correction. It will be made usage restriction.

Please inquire to our salesperson about details.