

# RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

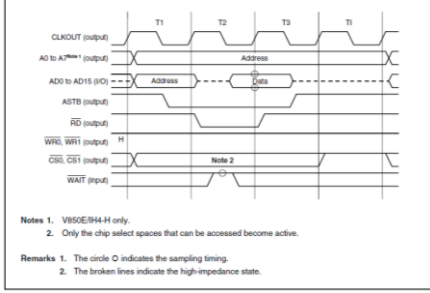
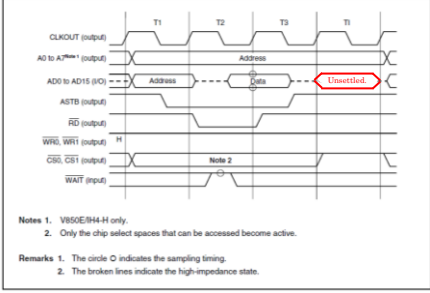
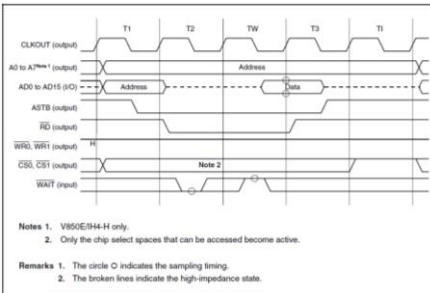
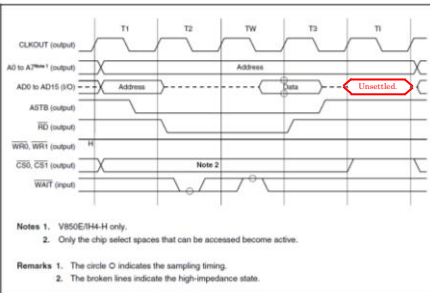
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|--------------------|---|----------|----------------------|---|------|------|
| Product Category   | MPU/MCU   |          | Document No.         | TN-V85-A020A/E  | Rev. | 1.00 |
| Title              | V850E/IG4-H,V850E/IH4-H Usage Restriction about bus control function. |          | Information Category | Usage Restriction   |      |      |
| Applicable Product | V850E/IG4-H,V850E/IH4-H series  | Lot No.  | Reference Document   | * V850E/IG4-H,V850E/IH4-H User's Manual: Hardware volume 3 (the 3rd edition)<br>R01UH0306EJ0300 |      |      |
|                    |   | All lots |                      |   |      |      |

A restriction matter of a bus control function was revealed about V850E/IG4-H, V850E/IH4-H

## 1. The detail of restriction

When using a bus control function, AD0-AD15 terminal becomes unsettled at idle State.

User's manual are corrected as follows.

| Item | Page | Correction point   | Current state.  | After restriction   |
|------|------|--|---|---|
| 1.   | 1148 | (1) bus cycle control register (BCC)                                 | <p>Cautions 1. The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to idle state insertion.</p> <p>2. Write to the BCC register after reset, and then do not change the set values. Also, when changing the initial values of the BSC register, do not access an external memory area until the settings are complete. However, it is possible to access external memory areas whose initialization settings are complete.</p> <p>3. The chip select signal (CSi) does not become active in the idle state (n = 0, 1).</p> | <p>Cautions 1. The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to idle state insertion.</p> <p>2. Write to the BCC register after reset, and then do not change the set values. Also, when changing the initial values of the BSC register, do not access an external memory area until the settings are complete. However, it is possible to access external memory areas whose initialization settings are complete.</p> <p>3. The chip select signal (CSi) does not become active in the idle state (n = 0, 1).</p> <p>4. AD0-AD15 pins will be unsettled output in the idle state.</p> |
| 2.   | 1153 | (3) Read cycle (When idle state insertion)                           | <p>(3) Read cycle (when idle state insertion)</p>  <p>Notes 1. V850E/IH4-H only.<br/>2. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p>   | <p>(3) Read cycle (when idle state insertion)</p>  <p>Notes 1. V850E/IH4-H only.<br/>2. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p>  |
| 4.   | 1154 | (4) Read cycle (When data wait state (1 wait), idle state insertion) | <p>(4) Read cycle (when data wait state (1 wait), idle state insertion)</p>  <p>Notes 1. V850E/IH4-H only.<br/>2. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p>   | <p>(4) Read cycle (when data wait state (1 wait), idle state insertion)</p>  <p>Notes 1. V850E/IH4-H only.<br/>2. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p>  |

| Item                  | Page       | Correction point  | Current state.  | After restriction     |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |
|-----------------------|------------|---|---|-----------------------|-----|-----|---------|-----------|-----------|--------|------------|-----------|---|-----------------------|-----|-----|---------|-----------|-----------|--------|------------|-----------|
| 5.                    | 1158       | (8) Write cycle (when idle state insertion)                           | <p>(8) Write cycle (when idle state insertion)</p> <p>Notes 1. V850E/H44-H only<br/>2. The levels of these signals are as follows, depending on the access data bus width.</p> <table border="1"> <thead> <tr> <th>Access Data Bus Width</th> <th>WRI</th> <th>WRG</th> </tr> </thead> <tbody> <tr> <td>16 bits</td> <td>Low level</td> <td>Low level</td> </tr> <tr> <td>8 bits</td> <td>High level</td> <td>Low level</td> </tr> </tbody> </table> <p>3. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p>                           | Access Data Bus Width | WRI | WRG | 16 bits | Low level | Low level | 8 bits | High level | Low level | <p>(8) Write cycle (when idle state insertion)</p> <p>Notes 1. V850E/H44-H only<br/>2. The levels of these signals are as follows, depending on the access data bus width.</p> <table border="1"> <thead> <tr> <th>Access Data Bus Width</th> <th>WRI</th> <th>WRG</th> </tr> </thead> <tbody> <tr> <td>16 bits</td> <td>Low level</td> <td>Low level</td> </tr> <tr> <td>8 bits</td> <td>High level</td> <td>Low level</td> </tr> </tbody> </table> <p>3. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p>                           | Access Data Bus Width | WRI | WRG | 16 bits | Low level | Low level | 8 bits | High level | Low level |
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| 16 bits               | Low level  | Low level   |   |                       |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |
| 8 bits                | High level | Low level   |   |                       |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |
| Access Data Bus Width | WRI        | WRG   |   |                       |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |
| 16 bits               | Low level  | Low level   |   |                       |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |
| 8 bits                | High level | Low level   |   |                       |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |
| 6.                    | 956        | (9) Write cycle (When data wait State (1 wait), idle state insertion) | <p>(9) Write cycle (when data wait state (1 wait), idle state insertion)</p> <p>Notes 1. V850E/H44-H only<br/>2. The levels of these signals are as follows, depending on the access data bus width.</p> <table border="1"> <thead> <tr> <th>Access Data Bus Width</th> <th>WRI</th> <th>WRG</th> </tr> </thead> <tbody> <tr> <td>16 bits</td> <td>Low level</td> <td>Low level</td> </tr> <tr> <td>8 bits</td> <td>High level</td> <td>Low level</td> </tr> </tbody> </table> <p>3. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p> | Access Data Bus Width | WRI | WRG | 16 bits | Low level | Low level | 8 bits | High level | Low level | <p>(9) Write cycle (when data wait state (1 wait), idle state insertion)</p> <p>Notes 1. V850E/H44-H only<br/>2. The levels of these signals are as follows, depending on the access data bus width.</p> <table border="1"> <thead> <tr> <th>Access Data Bus Width</th> <th>WRI</th> <th>WRG</th> </tr> </thead> <tbody> <tr> <td>16 bits</td> <td>Low level</td> <td>Low level</td> </tr> <tr> <td>8 bits</td> <td>High level</td> <td>Low level</td> </tr> </tbody> </table> <p>3. Only the chip select spaces that can be accessed become active.</p> <p>Remarks 1. The circle O indicates the sampling timing.<br/>2. The broken lines indicate the high-impedance state.</p> | Access Data Bus Width | WRI | WRG | 16 bits | Low level | Low level | 8 bits | High level | Low level |
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| 8 bits                | High level | Low level   |   |                       |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |
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| 8 bits                | High level | Low level   |   |                       |     |     |         |           |           |        |            |           |   |                       |     |     |         |           |           |        |            |           |

2. Workaround

When using the bus function, be careful so that a signal of AD0-AD15 terminal doesn't collide with idle state.

This issue is not planned for correction. It will be made usage restriction.

Please inquire to our salesperson about details.