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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A860A/E	Rev.	1.00
Title	User's Manuals Regarding CAN Module		Information Category	Technical Notification		
Applicable Product	SH72A2, SH72A0 Group	Lot No.	Reference Document	User's Manual: Hardware of Applicable Products		

This document describes corrections to the "CAN module" section in the User's Manual: Hardware of the above group.

The corrections are indicated in red below.

Page and section numbers are based on the SH72A2 Group, SH72A0 Group User's Manual: Hardware. Refer to the table on the final page for the corresponding pages and chapters in other groups.

<Correction>

- **Page 789 of 1118**

The description of BLIF Bit in 20.3.19 is corrected as follows;

Before correction

The BLIF bit is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the bit is set to 1, redetection takes place under either of the following conditions;

- After this bit is set to 0 from 1, recessive bits are detected.
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again.

After correction

The BLIF bit is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

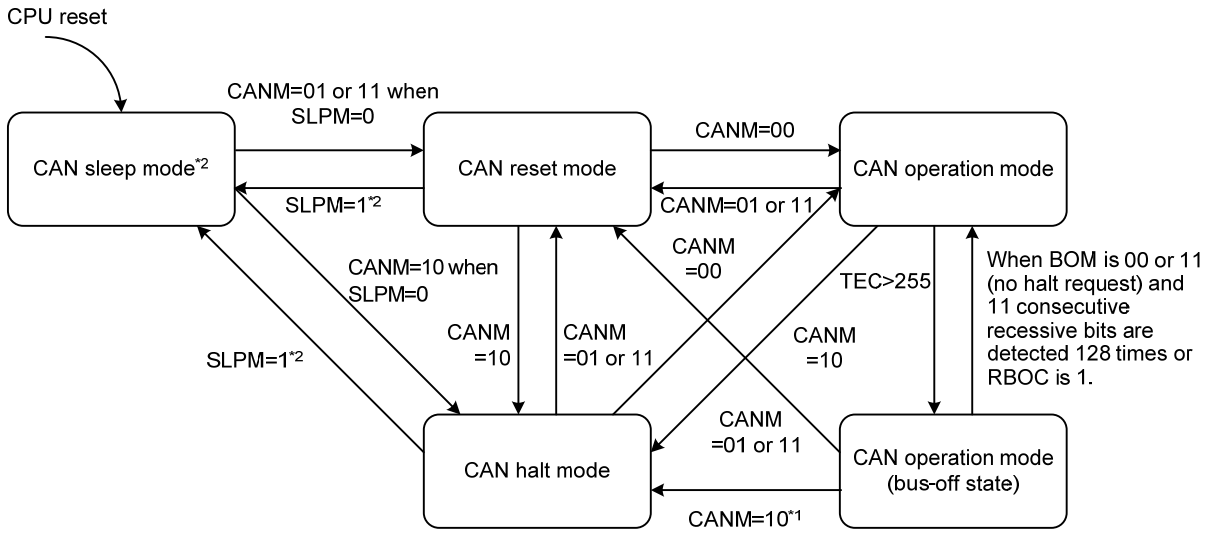
After the bit is set to 1, redetection of bus lock takes place under either of the following conditions;

- After this bit is set to 0 from 1, recessive bits are detected. (bus lock is released)
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again. (internal reset)

- **Page 796 of 1118**

Note 3 is added to Figure 20.9 as follows;

Before correction



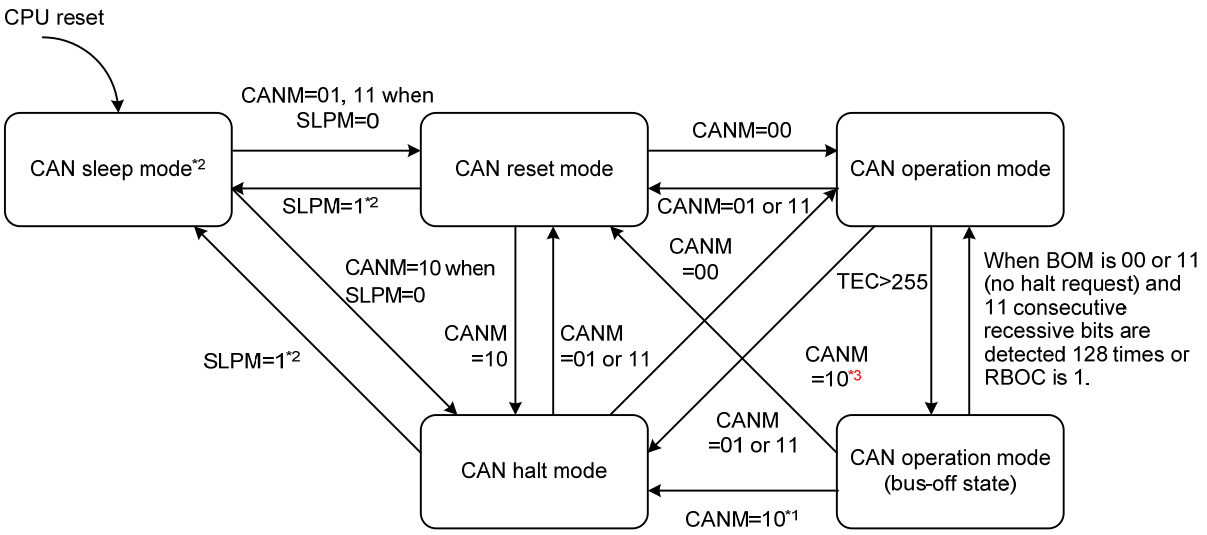
CANM, SLPM, BOM, RBOC: Bits in the CiCTLR register

Notes 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bits.
- When the BOM bits are 01, the state transition timing is immediately after entering the bus-off state.
- When the BOM bits are 10, the state transition timing is at the end of the bus-off state.
- When the BOM bits are 11, the state transition timing is at the setting of the CANM bits to 10 (CAN halt mode).

Notes 2. Write to the SLPM bit in CAN reset mode or CAN halt mode. When rewriting the SLPM bit, set only this bit to 0 or 1.

Figure 20.9 Transition between CAN Operating Modes (i=0 to 5)

After correction



CANM, SLPM, BOM, RBOC: Bits in the CiCTLR register

Notes 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bits.
- When the BOM bits are 01, the state transition timing is immediately after entering the bus-off state.
- When the BOM bits are 10, the state transition timing is at the end of the bus-off state.
- When the BOM bits are 11, the state transition timing is at the setting of the CANM bits to 10 (CAN halt mode).

Notes 2. Write to SLPM bit in CAN reset mode or CAN halt mode. When rewriting the SLPM bit, set only this bit to 0 or 1.

Notes 3. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Figure 20.9 Transition between CAN Operating Modes (i=0 to 5)

Table 20.15 is corrected as follows;

Before correction

Table 20.15 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode (forcible transition) CANM=11	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM=01	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission*1*4.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception*2*3.	CAN module enters CAN halt mode after waiting for the end of message transmission*1*4.	[When the BOM bits are 00] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bits are 01] CAN module enters automatically CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bits are 10] CAN module enters automatically CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bits are 11] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

Notes: BOM bits: Bits in the CiCTLR register (i=0 to 5)

1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in the CiEIFR register.
3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN mode transits to CAN halt mode.
4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN mode transits to the requested CAN mode.

After correction

Table 20.15 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode (forcible transition) CANM=11	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM=01	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission *1*4.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception *2*3.	CAN module enters CAN halt mode after waiting for the end of message transmission *1*2*4.	[When the BOM bits are 00] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bits are 01] CAN module enters automatically CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bits are 10] CAN module enters automatically CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bits are 11] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

Notes: BOM bits: Bits in the CiCTLR register (i=0 to 5)

1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the BLIF bit in the CiEIFR register. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN halt mode when the CAN bus is locked in dominant state.

4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN halt mode when the CAN bus is locked in dominant state.

<Reference Documents>

Applicable Product	Manual and Document Number	Page Number, Figure/Title Number		
		BLIF	Figure 20.9	Table 20.15
SH72A2 Group, SH72A0 Group	SH72A2 Group, SH72A0 Group User's Manual: Hardware Rev.1.00 (R01UH0164EJ0100)	Page 789 of 1118 20.3.19	Page 796 of 1118 Figure 20.9	Page 798 of 1118 Table 20.15