RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0109A/E	Rev.	1.00
Title	User's Manual Hardware correction : Modification of maximum transfer rate and access timing value for RSPI		Information Category	Technical Notification		
Applicable Product	RZ/G2L Group RZ/G2LC Group RZ/V2L Group RZ/G2UL Group RZ/A3UL Group RZ/Five Group	Lot No. All lots	Reference Document	RZ/G2L Group, RZ/G2LC Group, RZ/V2L Group User’s Manual: Hardware Rev.1.20 RZ/G2UL Group, RZ/A3UL Group, RZ/Five Group User’s Manual: Hardware Rev.1.10		

This technical update describes document corrections of the following User’s Manual: Hardware.

RZ/G2L Group, RZ/G2LC Group User’s Manual: Hardware Rev.1.20	(R01UH0914EJ0120)
RZ/V2L Group User’s Manual: Hardware Rev.1.20	(R01UH0936EJ0120)
RZ/G2UL Group User’s Manual: Hardware Rev.1.10	(R01UH0968EJ0110)
RZ/A3UL Group User’s Manual: Hardware Rev.1.10	(R01UH0973EJ0110)
RZ/Five Group User’s Manual: Hardware Rev.1.10	(R01UH0986EJ0110)

1. **Section 1. Overview,** the following description is fixed.

- **RZ/G2L,LC and RZ/V2L**
  - **1.2.12 Peripheral Module, Renesas Serial Peripheral Interface (RSPI)**

    [From] Maximum transfer rate: 50Mbps

    [To] ~~Maximum transfer rate: 50Mbps~~

- **RZ/G2UL and RZ/A3UL**
  - **1.2.11 Peripheral Module, Renesas Serial Peripheral Interface (RSPI)**

    [From] Maximum transfer rate: 33Mbps

    [To] ~~Maximum transfer rate: 33Mbps~~

- **RZ/Five**
  - **1.2.8 Peripheral Module, Renesas Serial Peripheral Interface (RSPI)**

    [From] Maximum transfer rate: 33Mbps

    [To] ~~Maximum transfer rate: 33Mbps~~

2. Section 24. Renesas Serial Peripheral Interface, the following description is fixed.

■ RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/A3UL and RZ/Five

- **24.3.8 Bit Rate Register (SPBR)**

[From]

Table 24.3 Relationship between SPBR and BRDV1 and BRDV0 Settings

SPBR (n)	BRDV[1:0] (N)	Division Ratio	Bit Rate P0ϕ = 100 MHz
0	0	2*1	50.00 Mbps
1	0	4	25.00 Mbps
2	0	6	16.67 Mbps
3	0	8	12.50 Mbps
4	0	10	10.00 Mbps
5	0	12	8.33 Mbps
5	1	24	4.17 Mbps
5	2	48	2.08 Mbps
5	3	96	1.04 Mbps
255	3	4096	24.41 Kbps

Note 1. Decide the bit rate to be actually used in the system considering timing specifications.

[To]

Table 24.3 Relationship between SPBR and BRDV1 and BRDV0 Settings

SPBR (n)	BRDV[1:0] (N)	Division Ratio	Bit Rate *1 P0ϕ = 100 MHz
0	0	~~2*1~~ 2	~~50.00 Mbps~~ Not Available
1	0	4	25.00 Mbps
2	0	6	16.67 Mbps
3	0	8	12.50 Mbps
4	0	10	10.00 Mbps
5	0	12	8.33 Mbps
5	1	24	4.17 Mbps
5	2	48	2.08 Mbps
5	3	96	1.04 Mbps
255	3	4096	24.41 Kbps

Note 1. Decide the bit rate to be actually used in the system considering timing specifications.

- **24.4.1 Overview of Operations**

[From]

Table 24.4 Relationship between Modes and SPCR and Description of Each Mode

Mode	Slave (SPI Operation)	Master (SPI Operation)
MSTR bit setting	0	1
MODFEN bit setting	0 or 1	0
RSPCK signal	Input	Output
MOSI signal	Input	Output
MISO signal	Output/Hi-Z	Input
SSL signal	Input	Output
SSL polarity modification function	Supported	Supported
Transfer rate	Up to P0ϕ/8	Up to P0ϕ/2
Clock source	RSPCK input	On-chip baud rate generator
Clock polarity	Two	Two
Clock phase	Two	Two
First transfer bit	MSB/LSB	MSB/LSB
Transfer data length	8, 16, or 32 bits	8, 16, or 32 bits
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0, 1)
RSPCK delay control	Not supported	Supported
SSL negation delay control	Not supported	Supported
Next-access delay control	Not supported	Supported
Transfer activation method	SSL input active or RSPCK oscillation	Transmit buffer is written when SPE = 1
Sequence control	Not supported	Supported
Transmit buffer empty detection	Supported	Supported
Receive buffer full detection	Supported	Supported
Overrun error detection	Supported	Not Supported
Mode fault error detection	Supported (MODFEN = 1)	Not supported

[To]

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Mode	Slave (SPI Operation)	Master (SPI Operation)
MSTR bit setting	0	1
MODFEN bit setting	0 or 1	0
RSPCK signal	Input	Output
MOSI signal	Input	Output
MISO signal	Output/Hi-Z	Input
SSL signal	Input	Output
SSL polarity modification function	Supported	Supported
Transfer rate	Up to P0ϕ/8	Up to P0ϕ/2 **(Up to P0ϕ/4 when P0ϕ is 100MHz)**
Clock source	RSPCK input	On-chip baud rate generator
Clock polarity	Two	Two
Clock phase	Two	Two
First transfer bit	MSB/LSB	MSB/LSB
Transfer data length	8, 16, or 32 bits	8, 16, or 32 bits
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0, 1)
RSPCK delay control	Not supported	Supported
SSL negation delay control	Not supported	Supported
Next-access delay control	Not supported	Supported
Transfer activation method	SSL input active or RSPCK oscillation	Transmit buffer is written when SPE = 1
Sequence control	Not supported	Supported
Transmit buffer empty detection	Supported	Supported
Receive buffer full detection	Supported	Supported
Overrun error detection	Supported	Not Supported
Mode fault error detection	Supported (MODFEN = 1)	Not supported

3. Section 48. Electrical Characteristics, the following acess timing value is fixed.

- **RZ/G2L,LC and RZ/V2L**
  - **48.5.20 Renesas Serial Peripheral Interface (RSPI) Access Timing**,

    Table 48.44 Renesas Serial Peripheral Interface Timing

    Data output delay time, Master, t_{OD}, Max

    [From] 21ns

    [To] 19ns

- **RZ/G2UL and RZ/A3UL**
  - **48.5.17 Renesas Serial Peripheral Interface (RSPI) Access Timing,**

    Table 48.41 Renesas Serial Peripheral Interface Timing

    Data output delay time, Master, t_{OD}, Max

    [From] 21ns

    [To] 19ns

- **RZ/Five**
  - **48.5.16 Renesas Serial Peripheral Interface (RSPI) Access Timing,**

    Table 48.41 Renesas Serial Peripheral Interface Timing

    Data output delay time, Master, t_{OD}, Max

    [From] 21ns

    [To] 19ns