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Renesas Electronics Corporation

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

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|------------------------------|-------------------------------------|-------------------------------|---|---|----------------|---|
| Classification of Production | Microprocessor | | No | TN-SH7-453A/E | Rev | 1 |
| THEME | Usage notices of the DMAC of SH7705 | Classification of Information | 1. Spec change 2. Supplement of Documents ③ 3. Limitation of Use 4. Change of Mask 5. Change of Production Line | | | |
| PRODUCT NAME | HD6417705 | Lot No. | Reference Documents | SH7705 Series Hardware Manual Rev.1.0 ADE-602-276 | Effective Date | |
| | | ALL | | | Eternity | |

Direct Memory Access Controller (DMAC) of SH7705 has following usage notes.

[Phenomenon]

If the following two conditions are satisfied simultaneously, DACK signal may be asserted illegally.

[Condition]

- (1) When the multiple DMA channels with the following setting operate simultaneously.
 - One DMA channel is set as burst mode and dual address mode with DACK output in write cycle.
 - Another DMA channel is set as cycle steal mode.
- (2) When DMAC can not acquire the bus mastership after burst transfer has completely finished (even if the next transfer request for cycle steal mode is accepted).

[Work around]

Don't set DMA transfer mode as (1).