

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

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Renesas Electronics Corporation

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# HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MPU		No	TN-SH7-341B/E	Rev	2 <sup>nd</sup>
THEME	Usage notice in power supply of SH7751 and SH7751R		Classification of Information	1. Spec change 2. Supplement of Documents ③ 3. Limitation of Use 4. Change of Mask 5. Change of Production Line		
PRODUCT NAME	SH7751, SH7751R	Lot No.	Reference Documents	SH7751 series Hardware manual	Effective Date	
		ALL			Eternity	

## 1. 1. Phenomenon

If the following condition (A) is not kept in supplying power, the clock may not be output correctly from the CKIO pin because PLL2 may oscillate abnormally.

Condition (A):

When VDDs (VDD, VDD-PLL1/2) are higher than 1.2V, VDDQs (VDDQ, VDD-CPG, VDD-RTC) must be higher than 2.0V.

## 2. Workaround

There are 3 workarounds to avoid this phenomenon.

- (1) Set the clock operation mode 6<sup>\*1</sup> in supplying power, and secure the condition (A), then set desired clock operation mode (shown in Figure 1).
- (2) Once start in the clock operation mode 6<sup>\*1</sup>, then set desired frequencies by changing FRQCR  
(The clock divider 1 can't be used in this clock operation mode).
- (3) Once stop PLL2 (to write 0 to FRQCR.PLL2EN), and keep the FRQCR.PLL2EN as 0 for more than 1us, then restart PLL2 (to write 1 to FRQCR.PLL2EN). (It is not guaranteed that the CKIO output is stable until this operation is finished. If you use this workaround, please check the noise or the clock network on the real board.)

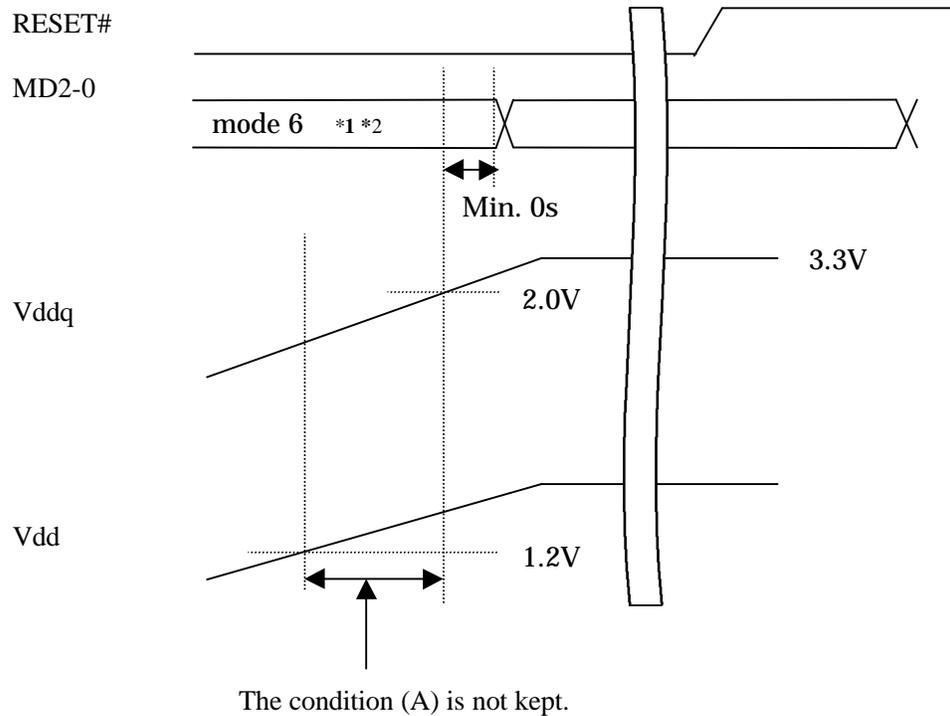


Figure 1. How to once set clock operation mode as mode 6.

\*1: Clock operation mode 6

(I)SH7751

- (1)MD0=Low, MD1=High, MD2=High
- (2)Divider 1=OFF, PLL1=Off, PLL2=OFF
- (3)Frequency (vs. EXTERNAL): CPU clock=1, Bus clock=1/2, Peripheral clock=1/2
- (4)EXTERNAL frequency range: 1~66.7MHz

(II)SH7751R

- (1)MD0=Low, MD1=High, MD2=High
- (2)PLL1=Off (x6), PLL2=OFF
- (3)Frequency (vs. EXTERNAL): CPU clock=1, Bus clock=1/2, Peripheral clock=1/2
- (4)EXTERNAL frequency range: 1~34MHz

\*2: Input high level to MD pins in compliance with the voltage level of the I/O, RTC, CPG power supply voltage.