To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A311A/E	Rev.	1.00
Title	Usage Notes on SSU for H8SX/1520 Group and H8SX/1582		Information Category	Technical Notification		
Applicable Product	H8SX/1520 Group H8SX/1582	Lot No. All lots	Reference Document	H8SX/1520 GroupHardware Manual (REJ09B0104-0200 Rev.2.00) H8SX/1582 Hardware Manual (REJ09B0199-0100Z Rev.1.00)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the usage note on SSU.

(1)Precaution on switching from transmission/reception operation to reception operation

(2)Precaution on DATS1/0 setting of SSCRL register

(3)Precaution on TXI Interrupt Setting

(1) Precaution on switching from transmission/reception operation to reception operation

P.14-29: "Figure 14.9 Flowchart Example of Simultaneous Transmission/Reception (SSU Mode)"
P.14-31: "Figure 14.17 Flowchart Example of Simultaneous Transmission/Reception (Clock Synchronous Communication Mode)"

If a switch from transmission/reception operation to reception operation is made during transmission/reception operation, the first reception might not operate properly. Therefore, the confirmation of the transmission completion (TEND=1 judgment) and the confirmation of the processing the final 1bit will be added. Please confirm the following flow chart for details.

The following precaution has already been described in the flowchart examples of data transmission in Figure 14.6, Figure 14.14.

<Content to be added>

Please setting according to the following procedures when switching from transmission or transmission/reception operation to reception operation.

① Wait until Transmission END (TEND) of SS status register (SSSR) are set(TEND=1, transmission completion)

② TEND is set to '0' after confirming transmission completion (TEND=1).

③ Wait until the final 1bit is processed, and then TE and RE of SS Enable Register (SSER) are set to '0'.

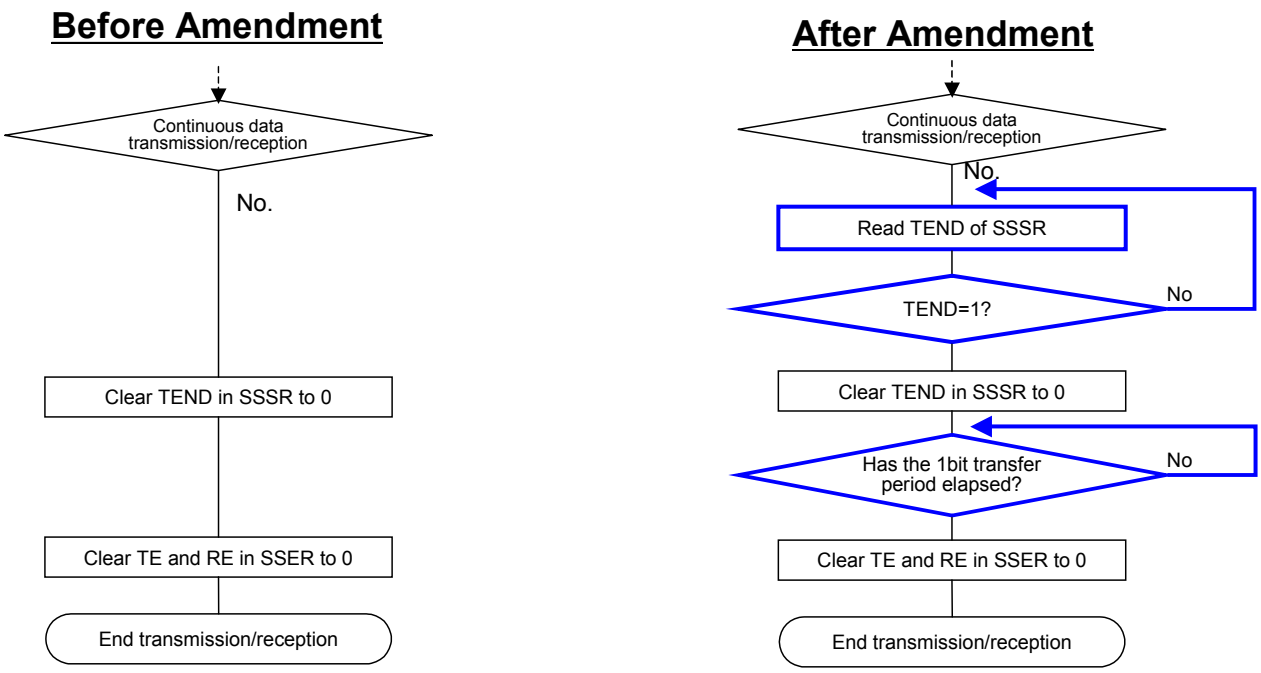

Figure 14.9, Figure 14.17 Example of Simultaneous Transmission/Reception Flowchart

(2) Precaution on DATS1/0 setting of SSCRL register

The communication might not be processed normally when disabled SSTDR or SSRDR registers, by the setting of the DATS bit in the SSCRL register that sets the transmission/reception data length, are accessed. Therefore, please don't access disabled SSTDR or SSRDR registers.

The following tables show the relation between the setting of the DATS bit and enabled/disabled SSTDR/SSRDR registers.

Correlation table of DATS bit setting and SSTDR

	DATS[1:0](SSCRL[1:0])			
SSTDR	00	01	10	11(Setting disable)
0	Enable	Enable	Enable	Disable
1	Disable	Enable	Enable	Disable
2	Disable	Disable	Enable	Disable
3	Disable	Disable	Enable	Disable

Correlation table of DATS bit setting and SSRDR

	DATS[1:0](SSCRL[1:0])			
SSRDR	00	01	10	11(Setting disable)
0	Enable	Enable	Enable	Disable
1	Disable	Enable	Enable	Disable
2	Disable	Disable	Enable	Disable
3	Disable	Disable	Enable	Disable

(3) Precaution on TXI Interrupt Setting

A not intended TXI interrupt might not be generated by setting in the way of the examples of initial settings, flowchart examples of data transmission, and flowchart example of simultaneous transmission/reception when the TXI interrupt is used in the transmission or the simultaneous transmission/reception in SSU.

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[Content]

In the H/W manual, when TXI interrupt is used for transmission or simultaneous transmission/reception, TIE bit and TE bit are set separately,

① TIE bit setting in example of initial setting (Figure14.4, Figure14.12)

② TE bit setting in the flowchart example of transmission or simultaneous transmission/reception (Figure14.6, Figure14.9, Figure14.14, Figure14.17)

In this setting, TIE bit of SSER register is set to “1” before setting TE bit of SSER register to “1” (transmission enabled), while the initial value of TDRE bit is “1”. This holds for the TXI interrupt condition (TIE=1 & TDRE=1).

Setting TE bit and TIE bit simultaneously can avoid this. Therefore the initial setting flow and flowchart will be changed.

Also SSCR2 will be set in the initial setting. SSCR2 setting is added to initial setting flowchart.

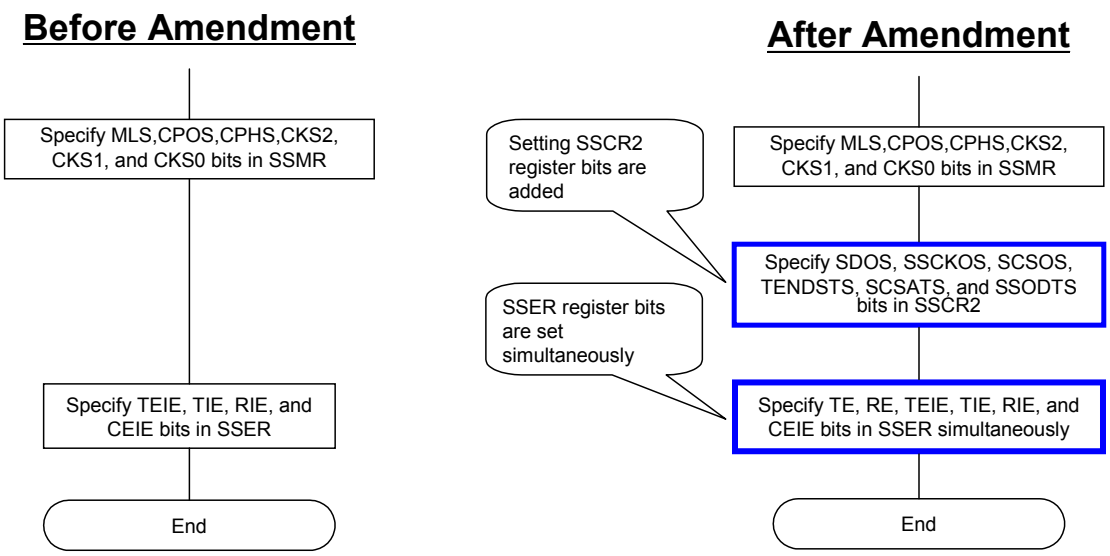
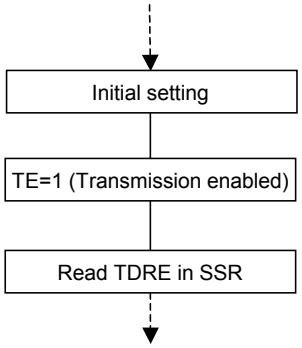


Figure 14.4 Example of Initial Settings in SSU Mode,

Figure 14.12 Example of Initial Settings in Clock Synchronous Communication Mode

Before Amendment



After Amendment

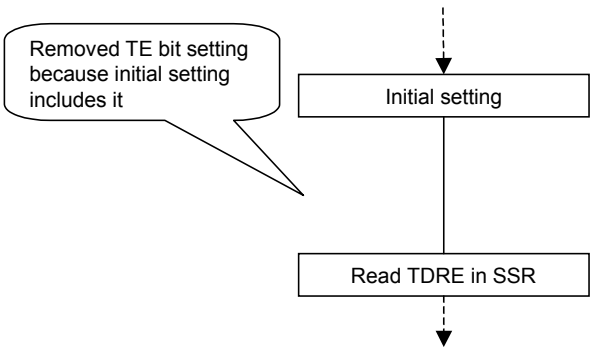
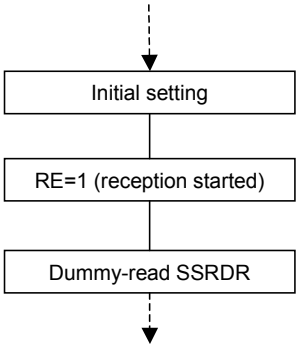


Figure 14.6, Figure 14.14 Flowchart Example of Data Transmission

Before Amendment



After Amendment

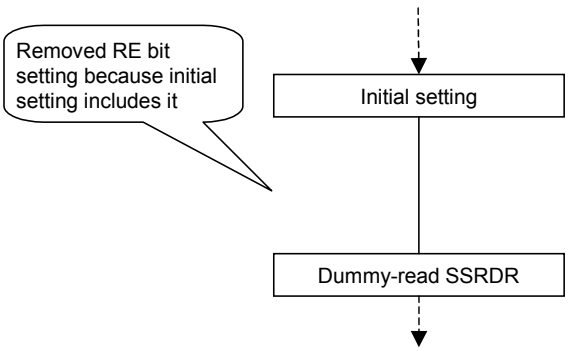
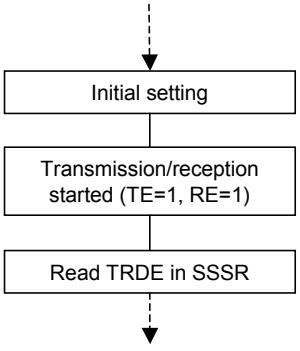


Figure 14.8, Figure 14.16 Flowchart Example of Data Reception

Before Amendment



After Amendment

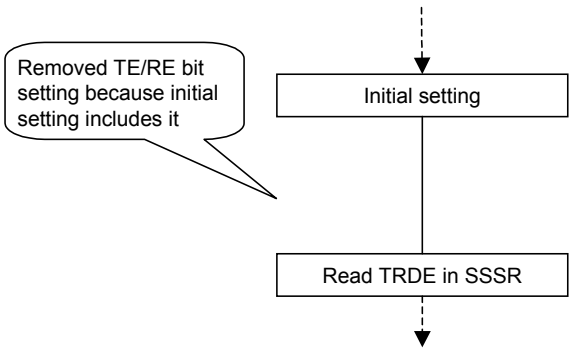


Figure14.9, Figure14.17 Flowchart Example of Data Transmission/Reception