Date: Jul. 20, 2022

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan Renesas Electronics Corporation

Product Category	System LSI		Document No.	TN-SH7-A0925A/E	Rev.	1.00
Title	Usage Notes for SH7786 Secondary Cache		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No. All Lots	Reference Document	SH7786 Group User's Manual: Hardw November 30, 2010 (REJ09B0501-0100)	are Rev.1	.00

rsı	um	m	aı	rv1
יטו	ulli		a	y j

Addition of Usage Notes for "SH7786 Group User's Manual: Hardware Rev.1.00".

[Priority level]

Importance: "Normal"

Urgency: "Normal"

[Web publication]

N/A (for specific users only)



RENESAS TECHNICAL UPDATE TN-SH7-A0925A/E

"This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. " (By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)							



Date: Jul. 20, 2022

[Correction]						
1. A.5.4 Usage Notes, Page 1979						
Current (from):						
None						

Correction (to):

(2) Note on Write to Memory-mapped OC address array or instruction OCBP

When the conditions in Figure A.14 are all satisfied, performance may decline due to L2 cache miss.

If there is a flow of "No", there is no problem.

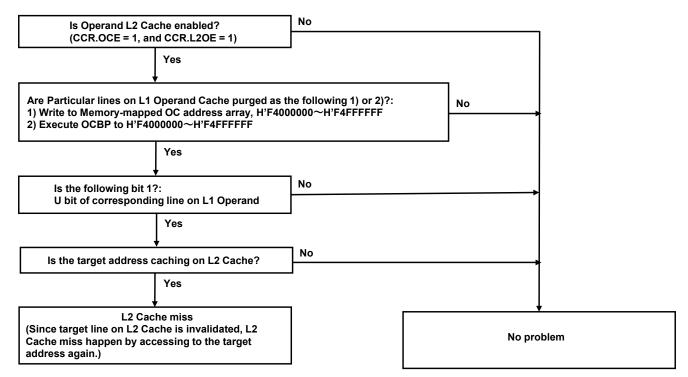


Figure A.14 Conditions in which L2 Cache miss happen

[Description]

Addition for Usage Notes about Write to Memory-mapped OC address or instruction OCBP.

[Reason for Correction]

For preventing performance declining due to L2 Cache miss.

- end of document -