RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	System LSI		Document No.	TN-SH7-A0924A/E	Rev.	1.00
Title	Usage Notes for SH7786 Secondary Cache		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No.	Reference Document	SH7786 Group User's Manual: Hardware Rev.1.00 November 30, 2010 (REJ09B0501-0100)		
		All Lots				

[Summary]

Addition of Usage Notes for "SH7786 Group User's Manual: Hardware Rev.1.00".

[Priority level]

Importance: **"Normal"**

Urgency: **"Normal"**

[Web publication]

N/A (for specific users only)

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[Correction]

1. A.5.4 Usage Notes, Page 1979

Current (from):

None

Correction (to):

A.5.4   Usage Notes

(1) L2 Cache control

Table A.12 below shows operational conditions of register setting and address restrictions of Operand and Instruction about L2 Cache control. The combination in Table A.12 should be followed so that L2 Cache can operate properly.

Table A.12 Operational conditions of L2 Cache control

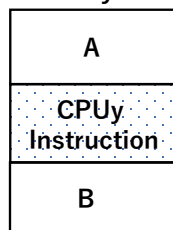| No	Used number of CPU	CPU0 L2OE	CPU0 L2IE	CPU1 L2OE	CPU1 L2IE	CPU0 Address restriction of Operand and Instruction	CPU1 Address restriction of Operand and Instruction
1	2	0	0	0	0	x	x
2		0	0	0	1	x	x
3		0	0	1	0	x	Figure A.13(1)
4		0	0	1	1	x	Figure A.13(1)
5		0	1	0	0	x	x
6		0	1	0	1	Figure A.13(2)	
7		0	1	1	0	Figure A.13(2)	
8		0	1	1	1	Figure A.13(2)	
9		1	0	0	0	Figure A.13(1)	x
10		1	0	0	1	Figure A.13(2)	
11		1	0	1	0	x	x
12		1	0	1	1	Figure A.13(2)	
13		1	1	0	0	Figure A.13(1)	x
14		1	1	0	1	Figure A.13(2)	
15		1	1	1	0	Figure A.13(2)	
16		1	1	1	1	Figure A.13(2)	
17	1	0	0	-	-	x	-
18		0	1	-	-	x	-
19		1	0	-	-	x	-
20		1	1	-	-	Figure A.13(1)	-
21		-	-	0	0	-	x
22		-	-	0	1	-	x
23		-	-	1	0	-	x
24		-	-	1	1	-	Figure A.13(1)

x: Don't care

-: Excluded

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The following condition should be satisfied:
  Area of Operand address [15:5] with CPUy (y: 0 or 1) does not overlap with one of CPUy Instruction but are located in area A or B.
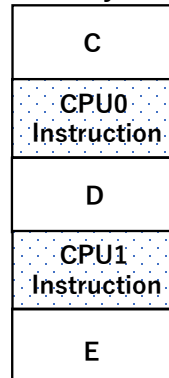
The following two conditions should be satisfied:
  1) Area of CPU0 Instruction does not overlap with one of CPU1 Instruction.
  2) Areas of Operand address [15:5] with CPU0 and CPU1 do not overlap with those of CPU0 and CPU1 Instruction but are located in area C or D or E.

Memory area

| A |
| CPUy Instruction |
| B |

Memory area

| C |
| CPU0 Instruction |
| D |
| CPU1 Instruction |
| E |

(1) Restriction of a CPU

(2) Restriction of two CPUs

Figure A.13 Address restriction of Operand and Instruction

[Description]

Addition for Usage Notes about L2 Cache Control.

[Reason for Correction]

For Description of proper operation for L2 Cache.

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