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RENESAS TECHNICAL UPDATE

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Product Category	System LSI		Document No.	TN-SH7-A0923A/E	Rev.	1.00
Title	Usage Notes for SH7786 Cache		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No. All Lots	Reference Document	SH7786 Group User's Manual: Hardware Rev.1.00 November 30, 2010 (REJ09B0501-0100)		

[Summary]

Addition of Usage Notes for “SH7786 Group User’s Manual: Hardware Rev.1.00”.

[Priority level]

Importance: **”Normal”**

Urgency: **”Normal”**

[Web publication]

N/A (for specific users only)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. A.3.6 Usage Notes, Page 1963

Current (from):

A.3.6 Usage Notes

(1) Sleep Mode

Before a CPU enters the sleep mode while coherency control is enabled for the CPU, all the entries of the OC and IC must be purged and invalidated, respectively. When a CPU enters the light sleep mode while coherency control is enabled for the CPU, it is not necessary for all the entries of the OC and IC to be purged and invalidated. In the light sleep mode, the coherency of the OC between the CPU and the other CPUs is maintained. When the ICBI instruction is executed while CCR.IBE is 1, IC invalidation is performed for CPUs that are in the light sleep mode.

(2) Share Data

In case of sharing data between the CPUs both of coherency control are disabled, or between the CPU which coherency control is enabled and the CPU which coherency control is disabled, a noncacheable area must be used.

Correction (to):

A.3.6 Usage Notes

(1) Sleep Mode

Before a CPU enters the sleep mode while coherency control is enabled for the CPU, all the entries of the OC and IC must be purged and invalidated, respectively. When a CPU enters the light sleep mode while coherency control is enabled for the CPU, it is not necessary for all the entries of the OC and IC to be purged and invalidated. In the light sleep mode, the coherency of the OC between the CPU and the other CPUs is maintained. When the ICBI instruction is executed while CCR.IBE is 1, IC invalidation is performed for CPUs that are in the light sleep mode.

(2) Share Data

In case of sharing data between the CPUs both of coherency control are disabled, or between the CPU which coherency control is enabled and the CPU which coherency control is disabled, a noncacheable area must be used.

(3) Cache coherency

When Operand Cache and Cache Coherency Control are enabled (CCR.OCE = 1 and CCR.CCD = 0) and instruction MOVCA is used, one of No.1 and No.2 in the table below should be satisfied.

Figure A.5A Operational conditions when instruction MOVCA is used.

No.	Operand Secondary Cache Enable: L2OE	Instruction OCBP	Instruction OCBI
1	1	Prohibit	Prohibit
2	0	Prohibit OCBP from writing to the area, H'F8000000 to H'F8FFFFFF	x

x: Don't care

[Description]

Addition for Usage Notes about Cache Coherency.

[Reason for Correction]

For description of operational conditions when Operand Cache and Cache Coherency Control are enabled.

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