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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A903A/E	Rev.	1.00
Title	Usage Notes on SCSPTR of Serial Communication Interface(SCI)		Information Category	Technical Notification		
Applicable Product	SH7147 Group	Lot No. All lots	Reference Document	SH7147 Group Hardware Manual Rev.3.00 (REJ09B0230-0300)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the correction of errors regarding SCSPTR Register of Serial Communication Interface (SCI) in the SH7147 Group Hardware Manuals as follows.

- 13.3.8 Serial Port Register (SCSPTR)

[Before correction]

Bit:	7	6	5	4	3	2	1	0
	EIO	-	-	-	SPB1IO	SPB1DT	SPB0IO	SPB0DT
Initial Value:	0	0	0	0	0	-	0	-
R/W:	R/W	-	-	-	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7	EIO	0	R/W	Error Interrupt Only Enables or disables RXI interrupts. While the EIO bit is set to 1, the SCI does not request an RXI interrupt to the CPU even if the RIE bit is set to 1. 0: The RIE bit enables or disables RXI and ERI interrupts. While the RIE bit is 1, RXI and ERI interrupts are sent to the INTC. 1: While the RIE bit is 1, only the ERI interrupt is sent to the INTC.
6 to 4	-	All 0	-	Reserved These bits are always read as 0. The write value should always be 0.
3	SPB1IO	0	R/W	Clock Port Input/Output in Serial Port Specifies the input/output direction of the SCK pin in the serial port. To output the data specified in the SPB1DT bit through the SCK pin as a port output pin, set the C/A bit in SCSMR and the CKE1 and CKE0 bits in SCSCR to 0. 0: Does not output the SPB1DT bit value through the SCK pin. 1: Outputs the SPB1DT bit value through the SCK pin.
2	SPB1DT	Undefined	R/W	Clock Port Data in Serial Port Specifies the data output through the SCK pin in the serial port. Output should be enabled by the SPB1IO bit (for details, refer to the SPB1IO bit description). When output is enabled, the SPB1DT bit value is output through the SCK pin. 0: Low level is output 1: High level is output

1	SPB0IO	0	R/W	Serial Port Break Input/Output Together with the SPB0DT bit and the TE bit in SCSCR, controls the TXD pin.
0	SPB0DT	Undefined	R/W	Serial Port Break Data Together with the SPB0IO bit and TE bit in SCSCR, controls the TXD pin. Note that the TXD pin function needs to have been selected with the pin function controller (PFC).

TE bit setting in SCSCR	SPB0IO bit setting	SPB0DT bit setting	State of TXD pin
0	0	*	SPB0DT output disabled (initial state)
0	1	0	Output, low level
0	1	1	Output, high level
1	*	*	Output for transmit data in accord with the serial core logic

Note: * Don't care

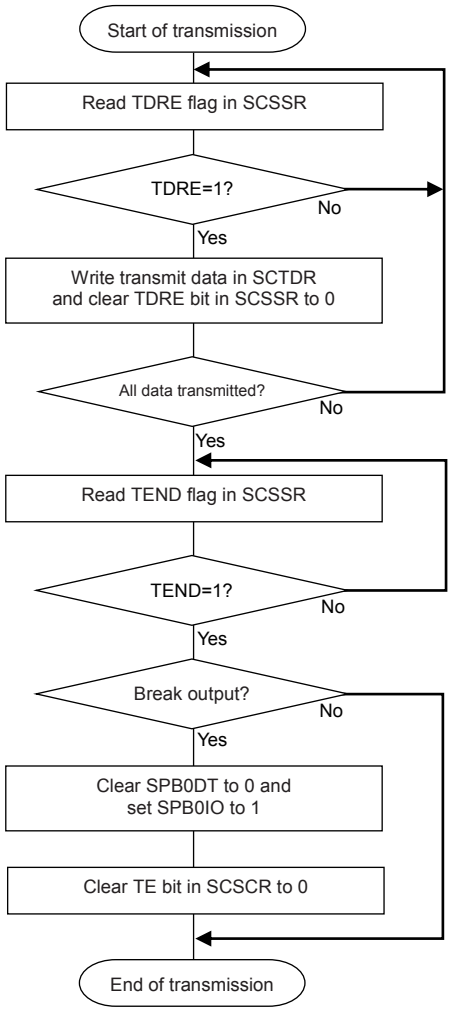
[After correction]

Bit:	7	6	5	4	3	2	1	0
	EIO	-	-	-	SPB1IO	SPB1DT	-	SPB0DT
Initial Value:	0	0	0	0	0	-	0	1
R/W:	R/W	-	-	-	R/W	W	-	W

Bit	Bit Name	Initial value	R/W	Description
7	EIO	0	R/W	Error Interrupt Only Enables or disables RXI interrupts. While the EIO bit is set to 1, the SCI does not request an RXI interrupt to the CPU even if the RIE bit is set to 1. 0: The RIE bit enables or disables RXI and ERI interrupts. While the RIE bit is 1, RXI and ERI interrupts are sent to the INTC. 1: While the RIE bit is 1, only the ERI interrupt is sent to the INTC.
6 to 4	-	All 0	-	Reserved These bits are always read as 0. The write value should always be 0.
3	SPB1IO	0	R/W	Clock Port Input/Output in Serial Port Specifies the input/output direction of the SCK pin in the serial port. To output the data specified in the SPB1DT bit through the SCK pin as a port output pin, set the C/A bit in SCSMR and the CKE1 and CKE0 bits in SCSCR to 0. 0: Does not output the SPB1DT bit value through the SCK pin. 1: Outputs the SPB1DT bit value through the SCK pin.
2	SPB1DT	Undefined	W	Clock Port Data in Serial Port Specifies the data output through the SCK pin in the serial port. Output should be enabled by the SPB1IO bit (for details, refer to the SPB1IO bit description). When output is enabled, the SPB1DT bit value is output through the SCK pin. 0: Low level is output 1: High level is output
1	-	0	-	Reserved
0	SPB0DT	1	W	Serial Port Break Data Together with the TE bit in SCSCR, controls the TXD pin. Note that the TXD pin function needs to have been selected with the pin function controller (PFC). This bit is a write-only bit and always read as an undefined value. TE bit setting in SCSCR / SPB0DT bit setting / State of TXD pin 0 / 0 / Output, low level 0 / 1 / Output, high level (Initial value) 1 / * / Output for transmit data Note: * Don't care

- Figure 13.4 Sample Flowchart for Transmitting Serial Data

[Before correction]



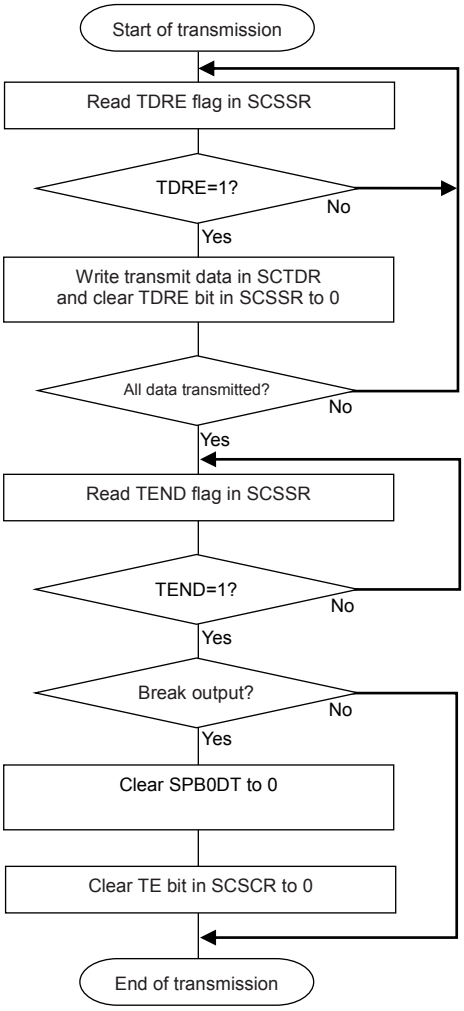
[1] SCI status check and transmit data write:
Read SCSSR and check that the TDRE flag is set to 1, then write transmit data to SCTDR, and clear the TDRE flag to 0.

[2] Serial transmission continuation procedure:
To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to SCTDR, and then clear the TDRE flag to 0.

Checking and clearing of the TDRE flag is automatic when the DTC is activated by a transmit data empty interrupt (TXI) request, and data is written to SCTDR.

[3] Break output at the end of serial transmission:
To output a break in serial transmission, clear the SPB0DT bit to 0 and set the SPB0IO bit to 1 in SCSPTR, then clear the TE bit in SCSCR to 0.

[After correction]



[1] SCI status check and transmit data write:
Read SCSSR and check that the TDRE flag is set to 1, then write transmit data to SCTDR, and clear the TDRE flag to 0.

[2] Serial transmission continuation procedure:
To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to SCTDR, and then clear the TDRE flag to 0.

Checking and clearing of the TDRE flag is automatic when the DTC is activated by a transmit data empty interrupt (TXI) request, and data is written to SCTDR.

[3] Break output at the end of serial transmission:
To output a break in serial transmission, clear the SPB0DT bit to 0 , then clear the TE bit in SCSCR to 0.

• Figure 13.20 SPBIO Bit, SPBDT Bit, and TXD Pin

[Before correction]

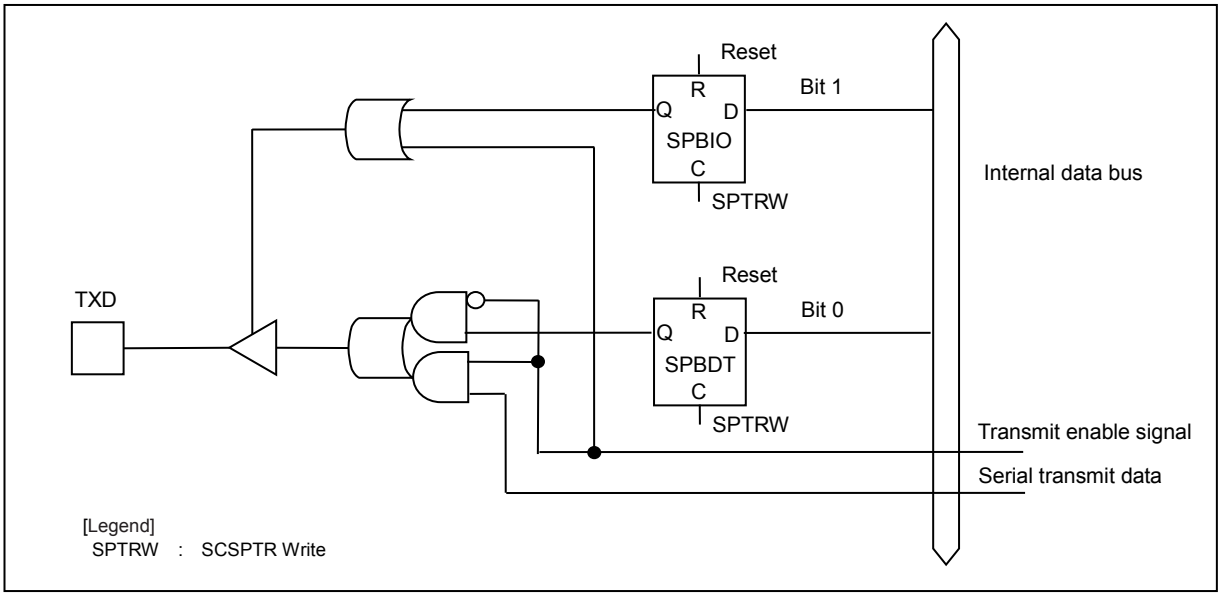


Figure 13.20 SPBIO Bit, SPBDT Bit and TXD Pin

[After correction]

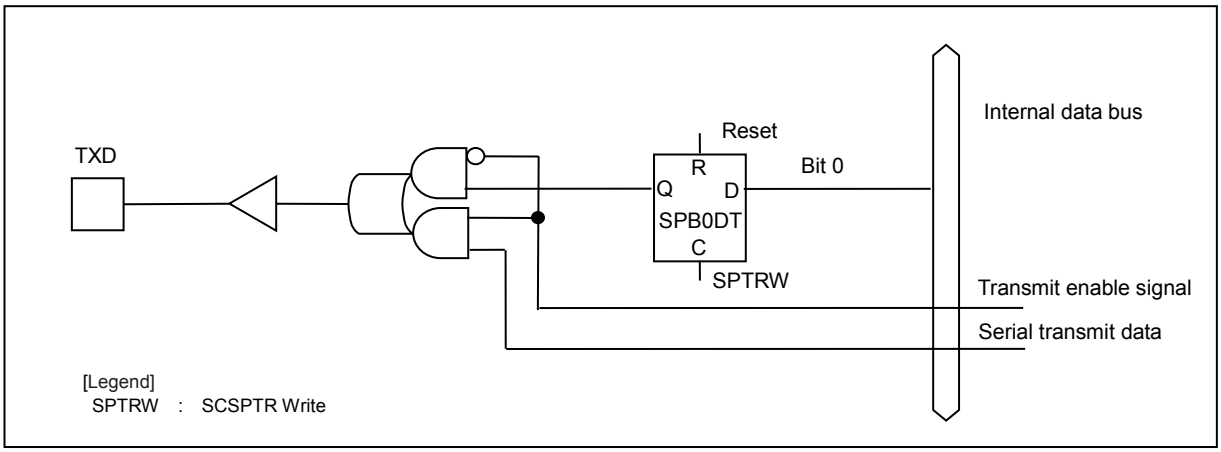


Figure 13.20 SPB0DT Bit and TXD Pin

- 13.7.4 Sending a Break Signal

[Before correction]

The I/O condition and level of the TXD pin are determined by the SPB0IO and SPB0DT bits in the serial port register (SCSPTR).

This feature can be used to send a break signal.

Until TE bit is set to 1 (enabling transmission) after initializing, TXD pin does not work.

During the period, mark status is performed by SPB0DT bit. Therefore, the SPB0IO and SPB0DT bits should be set to 1 (high level output).

To send a break signal during serial transmission, clear the SPB0DT bit to 0 (low level), then clear the TE bit to 0 (halting transmission).

When the TE bit is cleared to 0, the transmitter is initialized regardless of the current transmission state, and 0 is output from the TXD pin.

[After correction]

The output level of the TXD pin are determined by the SPB0DT bit in the serial port register (SCSPTR).

This feature can be used to send a break signal.

Until TE bit is set to 1 (enabling transmission) after initializing, TXD pin does not work.

During the period, mark status is performed by SPB0DT bit. Therefore, the SPB0DT bit should be set to 1 (high level).

To send a break signal during serial transmission, clear the SPB0DT bit to 0 (low level), then clear the TE bit to 0 (halting transmission).

When the TE bit is cleared to 0, the transmitter is initialized regardless of the current transmission state, and the level specified by the SPB0DT bit is output from the TXD pin.

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