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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A037A/E	Rev.	1.00
Title	Usage Notes for RZ/G1M PFC, SD Control Register Setting		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1M	Lot No. All lots	Reference Document	RZ/G1M User's Manual: Hardware Rev.1.00 Sep. 30, 2016 (R01UH0626EJ0100)		

There is a following document correction about the RZ/G series, RZ/G1M user's manual: hardware.

[Summary]

RZ/G1M User's manual: hardware usage notes for SD IO voltage settings.

[Products]

RZ/G1M

[Note]

There is no specification change (document correction only).

[Correction]

Section 5. Pin Function Controller (PFC)

Section 5.3.43 SD Control Register 6 (IOCTRL6)

(Gray part (abcd) are corrected or newly added)

Current (from):

Bit	Bit Name	Initial Value	R/W	Description
31	poc_sd0clk	1	R/W	Selecting IO voltage for the pin SD0_CLK 0: 1.8 V 1: 3.3 V
30	poc_sd0cmd	1	R/W	Selecting IO voltage for the pin SD0_CMD 0: 1.8 V 1: 3.3 V
29	poc_sd0dat0	1	R/W	Selecting IO voltage for the pin SD0_DATA0 0: 1.8 V 1: 3.3 V
28	poc_sd0dat1	1	R/W	Selecting IO voltage for the pin SD0_DATA1 0: 1.8 V 1: 3.3 V
27	poc_sd0dat2	1	R/W	Selecting IO voltage for the pin SD0_ DATA2 0: 1.8 V 1: 3.3 V

Bit	Bit Name	Initial Value	R/W	Description
26	poc_sd0dat3	1	R/W	Selecting IO voltage for the pin SD0_ DATA3 0: 1.8 V 1: 3.3 V
25	poc_sd0cd	1	R/W	Selecting IO voltage for the pin SD0_CD 0: 1.8 V 1: 3.3 V
24	poc_sd0wp	1	R/W	Selecting IO voltage for the pin SD0_WP 0: 1.8 V 1: 3.3 V
23	poc_sd2clk	1	R/W	Selecting IO voltage for the pin SD2_CLK 0: 1.8 V 1: 3.3 V
22	poc_sd2cmd	1	R/W	Selecting IO voltage for the pin SD2_CMD 0: 1.8 V 1: 3.3 V
21	poc_sd2dat0	1	R/W	Selecting IO voltage for the pin SD2_DATA0 0: 1.8 V 1: 3.3 V
20	poc_sd2dat1	1	R/W	Selecting IO voltage for the pin SD2_DATA1 0: 1.8 V 1: 3.3 V
19	poc_sd2dat2	1	R/W	Selecting IO voltage for the pin SD2_DATA2 0: 1.8 V 1: 3.3 V
18	poc_sd2dat3	1	R/W	Selecting IO voltage for the pin SD2_DATA3 0: 1.8 V 1: 3.3 V
17	poc_sd2cd	1	R/W	Selecting IO voltage for the pin SD2_CD 0: 1.8 V 1: 3.3 V
16	poc_sd2wp	1	R/W	Selecting IO voltage for the pin SD2_WP 0: 1.8 V 1: 3.3 V
15	poc_sd3clk	1	R/W	Selecting IO voltage for the pin SD3_CLK 0: 1.8 V 1: 3.3 V
14	poc_sd3cmd	1	R/W	Selecting IO voltage for the pin SD3_CMD 0: 1.8 V 1: 3.3 V
13	poc_sd3dat0	1	R/W	Selecting IO voltage for the pin SD3_DATA0 0: 1.8 V 1: 3.3 V
12	poc_sd3dat1	1	R/W	Selecting IO voltage for the pin SD3_DATA1 0: 1.8 V 1: 3.3 V
11	poc_sd3dat2	1	R/W	Selecting IO voltage for the pin SD3_DATA2 0: 1.8 V 1: 3.3 V
10	poc_sd3dat3	1	R/W	Selecting IO voltage for the pin SD3_DATA3 0: 1.8 V 1: 3.3 V

Bit	Bit Name	Initial Value	R/W	Description
9	poc_sd3cd	1	R/W	Selecting IO voltage for the pin SD3_CD 0: 1.8 V 1: 3.3 V
8	poc_sd3wp	1	R/W	Selecting IO voltage for the pin SD3_WP 0: 1.8 V 1: 3.3 V
7 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Correction (to):

Bit	Bit Name	Initial Value	R/W	Description
31	poc_sd0clk	1	R/W	Selecting IO voltage for the pin SD0 H'00: 1.8 V (VCCQ_SD0 = 1.8 V) H'FF: 3.3 V (VCCQ_SD0 = 3.3 V) Other than above: Setting prohibited Note. H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI (that can be used either 3.3V or 1.8V).
30	poc_sd0cmd	1	R/W	
29	poc_sd0dat0	1	R/W	
28	poc_sd0dat1	1	R/W	
27	poc_sd0dat2	1	R/W	
26	poc_sd0dat3	1	R/W	
25	poc_sd0cd	1	R/W	
24	poc_sd0wp	1	R/W	
23	poc_sd2clk	1	R/W	Selecting IO voltage for the pin SD2 H'00: 1.8 V (VCCQ_SD2 = 1.8 V) H'FF: 3.3 V (VCCQ_SD2 = 3.3 V) Other than above: Setting prohibited Note. H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI (that can be used either 3.3V or 1.8V).
22	poc_sd2cmd	1	R/W	
21	poc_sd2dat0	1	R/W	
20	poc_sd2dat1	1	R/W	
19	poc_sd2dat2	1	R/W	
18	poc_sd2dat3	1	R/W	
17	poc_sd2cd	1	R/W	
16	poc_sd2wp	1	R/W	
15	poc_sd3clk	1	R/W	Selecting IO voltage for the pin SD3 H'00: 1.8 V (VCCQ_SD3 = 1.8 V) H'FF: 3.3 V (VCCQ_SD3 = 3.3 V) Other than above: Setting prohibited Note. H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI (that can be used either 3.3V or 1.8V).
14	poc_sd3cmd	1	R/W	
13	poc_sd3dat0	1	R/W	
12	poc_sd3dat1	1	R/W	
11	poc_sd3dat2	1	R/W	
10	poc_sd3dat3	1	R/W	
9	poc_sd3cd	1	R/W	
8	poc_sd3wp	1	R/W	
7 to 0	—	All 0	R/W	—

Notes: 1. Any pin belongs to the same SD channel must be set to the same IO voltage as VCCQ_SDn. Even though setting different voltage for each pin of the same SD channel, it is impossible to change each pin voltage from the power supply voltage of the VCCQ_SDn.

2. When the VCCQ_SDn power supply voltage is 1.8-V to use the SDHI interface as SDR50/SDR104 mode or the GPIO (multiplexed with SDHI channel n pin) as 1.8-V IO, specify 1.8-V for IOCTRL6, then IO voltage of the SDHI channel n pins and multiplexed other function pins is all 1.8-V. In this condition, never input 3.3-V signal to these pins; if input 3.3-V signal, the LSI may be permanently damaged even though specifying the pin voltage to 3.3-V individually, furthermore, pull-up voltage of the unused pin which belongs to the same SD channel must be 1.8-V.

3. When the VCCQ_SDn power supply voltage is 3.3-V, to use the SDHI interface as default mode, high-speed mode or other module function, specify 3.3-V for IOCTRL6, then IO voltage of the SDHI channel n and multiplexed other

function pins is all 3.3-V. In this condition, output level of the pin is 3.3-V and if the external device can only operate with1.8-V, the external device may be permanently damaged even though specifying the pin voltage to 1.8-V individually.

4. For details of SDn related pin function settings, refer to following section.
   Section 5.3.8 GPSR6, 5.3.23 IPSR13, 5.3.24 IPSR14, 5.3.28 MOD_SEL2, 5.3.29 MOD_SEL3
5. Some of the following module pins are multiplexed with the SDn pins. They cannot be used with 1.8-V power supply (VCCQ_SDn) except for the multiplexed GPIO. Use them with 3.3-V power supply and set the corresponding VCCQ_SDn supply voltage to 3.3-V by IOCTRL6.
   CAN0(F), I2C1(C), IIC1(C), MMC, MMC(B), PWM0, PWM1(B), QSPI(B), SCIF3(C), SCIF5(B, C), TPU0.
   For details of multiplexed pins of SDn, refer to Table 4.1, List of Multiplexed Pin Functions in section 4, Pin Multiplexing.
6. To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

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