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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A885A/E	Rev.	1.00
Title	Usage Notes on the Multi-Function Timer Pulse Unit 2 (MTU2, MTU2S)		Information Category	Technical Notification		
Applicable Product	See below	Lot No. ALL	Reference Document	See below		

We would like to inform you of some points on usage of the multi-function timer pulse unit 2 (MTU2, MTU2S). When using this module, please apply the countermeasures listed below. The descriptions in the manual will be corrected in accord with these notes. The corrections are explained using the SH7280 Group, SH7243 Group User's Manual: Hardware as a representative example.

1. Timer Output Master Enable Register (TOER)

1.1 Usage Note

When the corresponding bit in TOER is changed from 1 (MTU output enabled) to 0 (MTU output disabled) while TCNT_3/4 is operating, a PWM waveform with a duty cycle different from that set up by the settings may be output when the corresponding bit is set to 1 again. Therefore, be sure to stop TCNT_3/4 first before changing a bit in TOER to 0.

1.2 Countermeasure

When a bit in TOER is changed from 1 to 0 after TCNT_3/4 is started, follow the procedure below.

(1) Set the bit in the timer start register (TSTR) that corresponds to the counter to 0 (which stops counting).

(2) Set the bit in TOER to 0.

1.3 Correction in the Manual

11.3.19 Timer Output Master Enable Register (TOER)

[Before correction (p.509)]

TOER is an 8-bit readable/writable register that enables/disables output settings for output pins TIOC4D, TIOC4C, TIOC3D, TIOC4B, TIOC4A, and TIOC3B. These pins do not output correctly if the TOER bits have not been set. Set TOER of CH3 and CH4 prior to setting TIOR of CH3 and CH4.

[After correction (p.509)]

TOER is an 8-bit readable/writable register that enables/disables output settings for output pins TIOC4D, TIOC4C, TIOC3D, TIOC4B, TIOC4A, and TIOC3B. These pins do not output correctly if the TOER bits have not been set. Set TOER of CH3 and CH4 prior to setting TIOR of CH3 and CH4. Set TOER when count operation of TCNT channels 3 and 4 is halted (See figures 11.35 and

11.38).

2. Timer Output Control Register 1 (TOCR1), Timer Output Control Register 2 (TOCR2)

2.1 Usage Note

When dead time is not to be generated, the level of the inverse-phase output is the exact inverse of the positive-phase output. At this time, only the OLSP bit is valid in TOCR1, and the value of the OLSN bit is ignored. In addition, only the OLSiP bit (i = 1 to 3) is valid in TOCR2, and the value of the OLSiN bit is ignored.

2.2 Correction in the Manual

11.3.20 Timer Output Control Register 1 (TOCR1)

[Before correction (p.510)]

Bit:	7	6	5	4	3	2	1	0
	-	PSYE	-	-	TOCL	TOCS	OLSN	OLSP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R/(W)*	R/W	R/W	R/W

Note: * This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to the bit.

Bit	Bit Name	Initial value	R/W	Description
3	TOCL	0	R/(W)*	TOC Register Write Protection*1 This bit selects the enable/disable of write access to the TOCS, OLSN, and OLSP bits in TOCR1. 0: Write access to the TOCS, OLSN, and OLSP bits is enabled 1: Write access to the TOCS, OLSN, and OLSP bits is disabled
2	TOCS	0	R/W	TOC Select This bit selects either the TOCR1 or TOCR2 setting to be used for the output level in complementary PWM mode and reset-synchronized PWM mode. 0: TOCR1 setting is selected 1: TOCR2 setting is selected
1	OLSN	0	R/W	Output Level Select N*2 This bit selects the reverse phase output level in reset-synchronized PWM mode/complementary PWM mode. See table 11.30.
0	OLSP	0	R/W	Output Level Select P*2 This bit selects the positive phase output level in reset-synchronized PWM mode/complementary PWM mode. See table 11.31.

Notes: 1. Setting the TOCL bit to 1 prevents accidental modification when the CPU goes out of control.
2. Clearing the TOCS0 bit to 0 makes this bit setting valid.

[After correction (p.510)]

Bit:	7	6	5	4	3	2	1	0
	-	PSYE	-	-	TOCL	TOCS	OLSN	OLSP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R/(W)*	R/W	R/W	R/W

Note: * This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to the bit.

Bit	Bit Name	Initial value	R/W	Description
3	TOCL	0	R/(W)*1	TOC Register Write Protection*2 This bit selects the enable/disable of write access to the TOCS, OLSN, and OLSP bits in TOCR1. 0: Write access to the TOCS, OLSN, and OLSP bits is enabled 1: Write access to the TOCS, OLSN, and OLSP bits is disabled
2	TOCS	0	R/W	TOC Select This bit selects either the TOCR1 or TOCR2 setting to be used for the output level in complementary PWM mode and reset-synchronized PWM mode. 0: TOCR1 setting is selected 1: TOCR2 setting is selected
1	OLSN	0	R/W	Output Level Select N*3*4 This bit selects the reverse phase output level in reset-synchronized PWM mode/complementary PWM mode. See table 11.30.
0	OLSP	0	R/W	Output Level Select P*3*4 This bit selects the positive phase output level in reset-synchronized PWM mode/complementary PWM mode. See table 11.31.

Notes:
1. This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to the bit.
2. Setting the TOCL bit to 1 prevents accidental modification when the CPU goes out of control.
3. Clearing the TOCS bit to 0 makes this bit setting valid.
4. The inverse-phase output is the exact inverse of the positive-phase output unless dead time is generated. When no dead time is generated, only the OLSP setting is valid.

11.3.21 Timer Output Control Register 2 (TOCR2)

[Before correction (p.513)]

Bit	Bit Name	Initial value	R/W	Description
7, 6	BF[1:0]	00	R/W	TOLBR Buffer Transfer Timing Select These bits select the timing for transferring data from TOLBR to TOCR2. For details, see table 11.32.
5	OLS3N	0	R/W	Output Level Select 3N* This bit selects the output level on TIOC4D in reset-synchronized PWM mode/complementary PWM mode. See table 11.33.
4	OLS3P	0	R/W	Output Level Select 3P* This bit selects the output level on TIOC4B in reset-synchronized PWM mode/complementary PWM mode. See table 11.34.
3	OLS2N	0	R/W	Output Level Select 2N* This bit selects the output level on TIOC4C in reset-synchronized PWM mode/complementary PWM mode. See table 11.35.
2	OLS2P	0	R/W	Output Level Select 2P* This bit selects the output level on TIOC4A in reset-synchronized PWM mode/complementary PWM mode. See table 11.36.
1	OLS1N	0	R/W	Output Level Select 1N* This bit selects the output level on TIOC3D in reset-synchronized PWM mode/complementary PWM mode. See table 11.37.
0	OLS1P	0	R/W	Output Level Select 1P* This bit selects the output level on TIOC3B in reset-synchronized PWM mode/complementary PWM mode. See table 11.38.

Note: * Setting the TOCS bit in TOCR1 to 1 makes this bit setting valid.

[After correction (p.513)]

Bit	Bit Name	Initial value	R/W	Description
7, 6	BF[1:0]	00	R/W	TOLBR Buffer Transfer Timing Select These bits select the timing for transferring data from TOLBR to TOCR2. For details, see table 11.32.
5	OLS3N	0	R/W	Output Level Select 3N*1*2 This bit selects the output level on TIOC4D in reset-synchronized PWM mode/complementary PWM mode. See table 11.33.
4	OLS3P	0	R/W	Output Level Select 3P*1*2 This bit selects the output level on TIOC4B in reset-synchronized PWM mode/complementary PWM mode. See table 11.34.
3	OLS2N	0	R/W	Output Level Select 2N*1*2 This bit selects the output level on TIOC4C in reset-synchronized PWM mode/complementary PWM mode. See table 11.35.
2	OLS2P	0	R/W	Output Level Select 2P*1*2 This bit selects the output level on TIOC4A in reset-synchronized PWM mode/complementary PWM mode. See table 11.36.
1	OLS1N	0	R/W	Output Level Select 1N*1*2 This bit selects the output level on TIOC3D in reset-synchronized PWM mode/complementary PWM mode. See table 11.37.
0	OLS1P	0	R/W	Output Level Select 1P*1*2 This bit selects the output level on TIOC3B in reset-synchronized PWM mode/complementary PWM mode. See table 11.38.

Notes: 1. Setting the TOCS bit in TOCR1 to 1 makes this bit setting valid.
2. The inverse-phase output is the exact inverse of the positive-phase output unless dead time is generated. When no dead time is generated, only the OLSiP setting is valid.

3. Connection of Cascaded Operation

3.1 Usage Note

In the case of simultaneous input capture to TCNT_1 and TCNT_2 during cascaded operation, the signals on the corresponding input pins can be selected as input-capture conditions. In this case, the input-capture condition is an edge of the signal obtained by taking the logical OR of the two input signals. Accordingly, if the level of either signal changes while the other is being driven high, input capture does not proceed.

3.2 Correction in the Manual

11.4.4 Cascaded Operation

[Before correction (p.542)]

For simultaneous input capture of TCNT_1 and TCNT_2 during cascaded operation, additional input capture input pins can be specified by the input capture control register (TICCR). For input capture in cascade connection, refer to section 11.7.22, Simultaneous Capture of TCNT_1 and TCNT_2 in Cascade Connection.

[After correction (p.542)]

For simultaneous input capture of TCNT_1 and TCNT_2 during cascaded operation, additional input capture input pins can be specified by the input capture control register (TICCR). Edge detection as the condition for input capture is the detection of edges in the signal produced by taking the logical OR of the signals on the main and additional pins. For details, refer to (4), Cascaded Operation Example (c). For input capture in cascade connection, refer to section 11.7.22, Simultaneous Capture of TCNT_1 and TCNT_2 in Cascade Connection.

11.4.4 Cascaded Operation

(4) Cascaded Operation Example (c)

[Before correction (p.545)]

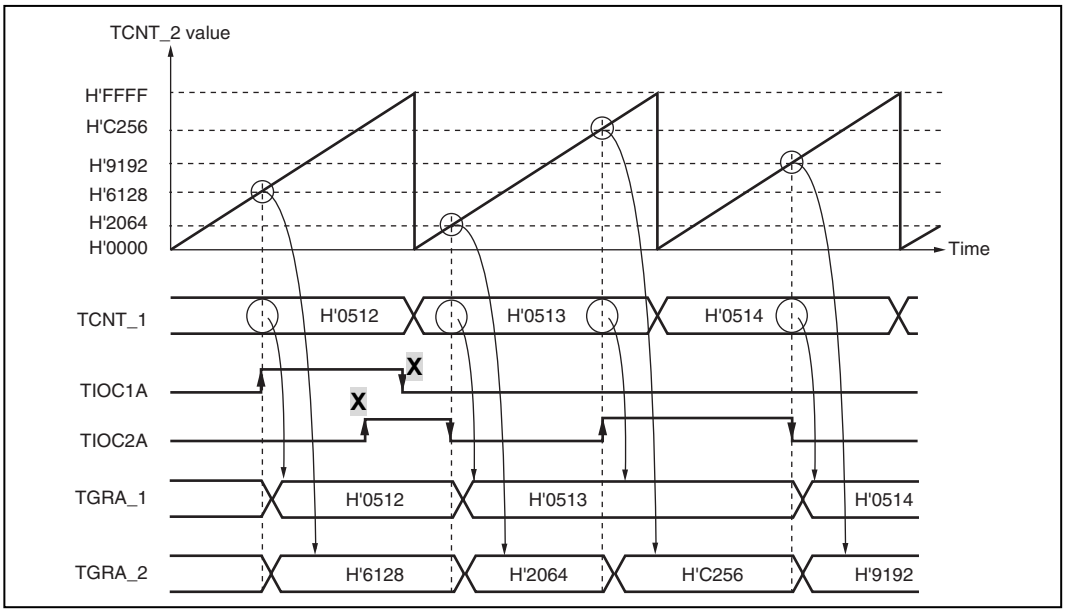

Figure 11.23 Cascaded Operation Example (c)

[After correction (p.545)]

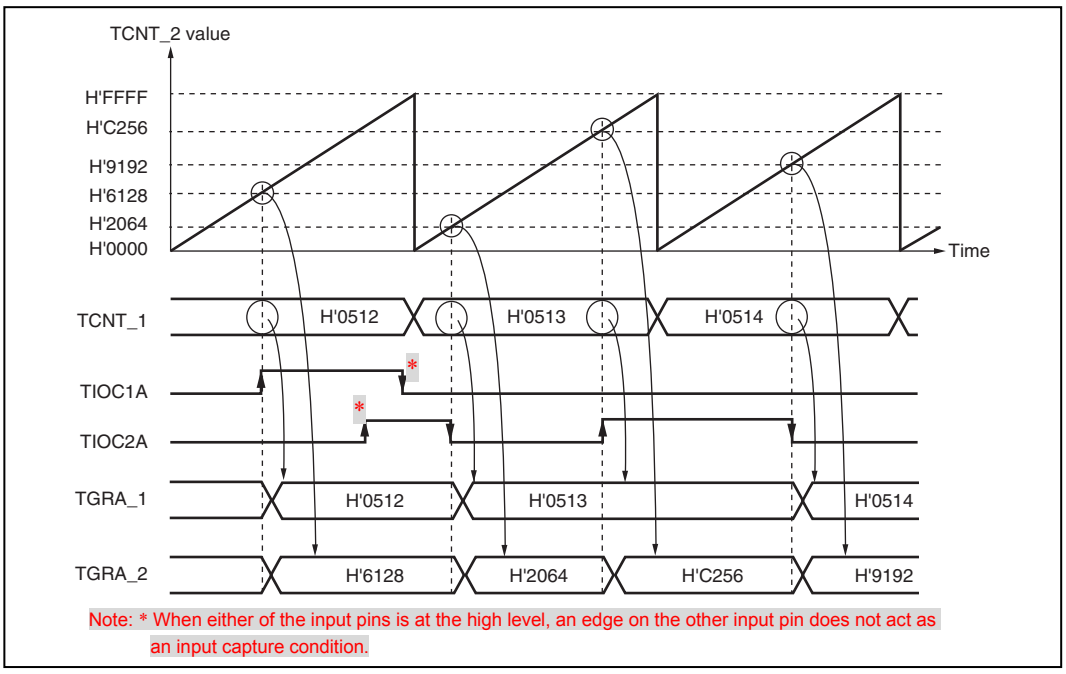

Figure 11.23 Cascaded Operation Example (c)

4. Compare Match in Channel 5

4.1 Usage Note

The compare match in channel 5 is generated even though the TCNTU/V/W_5 count operation is stopped.

4.2 Correction in the Manual

11.6.2 Interrupt Signal Timing

(1) TGF Flag Setting Timing in Case of Compare Match

[Before correction (p.637)]

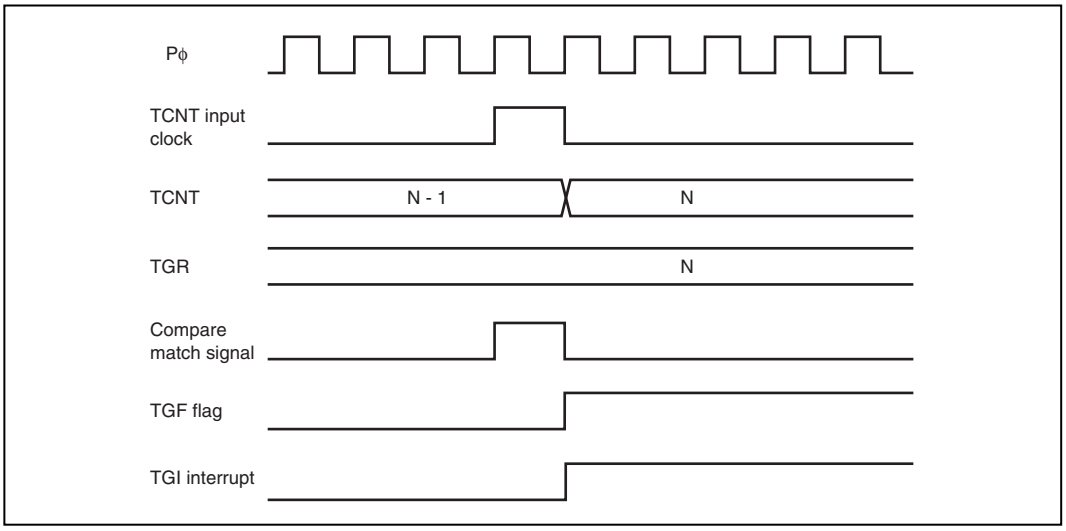

Figure 11.110 TGI Interrupt Timing (Compare Match) (Channel 5)

[After correction (p.637)]

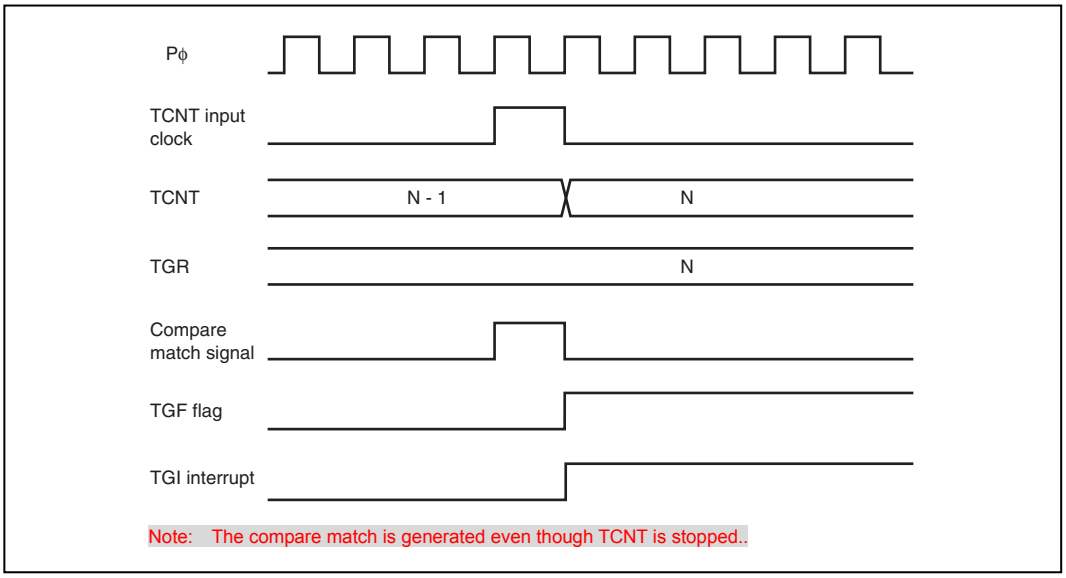

Figure 11.110 TGI Interrupt Timing (Compare Match) (Channel 5)

Applicable Products and Reference Documents

Series	Group	Reference Document Title	Rev.	Document No.
SH7080	SH7083, SH7084, SH7085, SH7086	SH7080 Group User's Manual: Hardware	5.00	R01UH0198EJ0500
SH7137	SH7131, SH7132, SH7136, SH7137	SH7137 Group Hardware Manual	3.00	REJ09B0402-0300
SH7146	SH7146, SH7149	SH7146 Group User's Manual: Hardware	4.00	R01UH0049EJ0400
SH7210	SH7211	SH7211 Group Hardware Manual	3.00	REJ09B0344-0300
SH7216	SH7214, SH7216	SH7214 Group, SH7216 Group User's Manual: Hardware	4.00	R01UH0230EJ0400
SH7231	SH7231	SH7231 Group User's Manual: Hardware	2.00	R01UH0073EJ0200
SH7239	SH7237, SH7239	SH7239 Group, SH7237 Group User's Manual: Hardware	2.00	R01UH0086EJ0200
SH7243	SH7243	SH7280 Group, SH7243 Group User's Manual: Hardware	3.00	R01UH0229EJ0300
SH7280	SH7285, SH7286	SH7280 Group, SH7243 Group User's Manual: Hardware	3.00	R01UH0229EJ0300
SH/Tiny	SH7124, SH7125	SH7125 Group, SH7124 Group Hardware Manual	5.00	REJ09B0243-0500