To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A358A/E	Rev.	1.00
Title	Usage notes on I^2C bus interface 2 (IIC2) in multi-master operation and master receive mode		Information Category	Technical Notification		
Applicable Product	H8/38776 Group	Lot No. All	Reference Document	H8/38776 Group Hardware manual (REJ09B0348-0100)		

Addition of I^2C bus interface 2 (IIC2) Usage note on H8/38776 group Hardware manual.
Please refer to following for details.

[Additional part] H8/38776 Group Hardware manual (Page 437 of 568)

3 . Restriction on Setting of Transfer Rate in Use of Multi-Master

In multi-master usage when the IIC transfer rate setting of this LSI is lower than those of the other masters, unexpected Length of SCL may occasionally be output. To avoid this, the specified value must be greater than or equal to the value Produced by multiplying the fastest transfer rate among the other masters by 1/1.8. For example, when the transfer rate of the fastest bus master among the other bus masters is 400 kbps, the transfer rate of the IIC of this LSI must be set to at least 223 kbps (=400/1.8)

4 . Restriction on Use of Bit Manipulation Instructions to Set MST and TRS when Multi-Master is Used

When master transmission is selected by consecutively manipulating the MST and TRS bits in multi-master usage, an arbitration loss during execution of the bit-manipulation instruction for TRS leads to the contradictory situation where AL in ICSR is 1 in master transmit mode (MST = 1, TRS = 1).

Ways to avoid this effect are listed below.

- Use the MOV instruction to set MST and TRS in multi-master usage.
- When arbitration is lost, confirm that MST = 0 and TRS = 0. If the setting of MST = 0 and TRS = 0 is not confirmed, set MST = 0 and TRS = 0 again.

5 . Usage Note on Master Receive Mode

In master receive mode, when SCL is fixed low on the falling edge of the 8th clock while the RDRF bit is set to 1 and ICDRR is read around the falling edge of the 8th clock, the clock is only fixed low in the 8th clock of the next round of data reception. The SCL is then released from its fixed state without reading ICDRR and the 9th clock is output. As a result, some receive data is lost.

Ways to avoid this effect are listed below.

- Read ICDRR in master receive mode before the rising edge of the 8th clock.
- Set RCVD to 1 in master receive mode and perform communication in units of one byte.