To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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RENESAS TECHNICAL UPDATE

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Product Category	MPU MCU		Document No.	TN-H8*-A402A/E	Rev.	1.00
Title	Usage Notes on H8S/20103, H8S/20203, H8S/20223 Group Products		Information Category	Technical Notification		
Applicable Product	H8S/20103, H8S/20203, H8S/20223 Groups	Lot No. All lots	Reference Document	H8S/20103, H8S/20203, H8S/20223 Group Hardware Manual Rev.1.00 (REJ09B0465-0100)		

We would like to inform you of the following points for caution in usage of H8S/20103, H8S/20203, H8S/20223 Group products.

1. Flash ROM

If the user ROM area is to be read while software commands are enabled (the value of FMCMDEN bit in FLMCR1 is 1) and the reprogramming mode is EW0, set the bus master operation clock φs to a frequency below 5 MHz.

2. Watchdog Timer

Only write values to the timer mode register WD (TMWD) of the watchdog timer while the bus master operation clock φs is not being frequency-divided (the value of the PHIS[2:0] bits in the power-down control register 3 (LPCR3) is B'000).

3. Sampling Circuit for Noise Canceler in φ sub clock

If the setting of the SUBNC[1:0] bits in SYSCCR is made to select usage of the sampling circuit of the noise canceler for the φsub clock , only enable the sampling circuit after completion of switching of the system clock from φloco to φosc. If the sampling circuit is enabled while the system clock is φloco, the supply of φ sub clock will be stopped during the period of waiting for stable φosc oscillation when the system clock is switched from φloco to φosc.

Furthermore, if an application is also using the sampling circuit of the noise canceler for the φ sub clock in the period of switching of the system clock signal between φlow and φosc, disable the sampling circuit of the noise canceler for the φ sub clock while φlow remains in use as the system clock.

4. Backup Function for External Clock Signals

When the backup function for external clock signals is to be used, switch the system clock from φloco to φosc before enabling the backup function. If enabling of the backup function is followed by switching of the system clock from φloco to φosc, switching of the clock signal may fail due to erroneous detection by the clock-stop detection circuit. Furthermore, if an application is also using the backup function in the period of switching of the system clock signal between φlow and φosc, disable the backup function while φlow is in use as the system clock signal. There are two procedures for enabling the backup function, with the appropriate selection depending on the method used to switch the system clock signal. Flowcharts for the two procedures are given on the following pages.

(1) Figure 1 is a flowchart of the procedure for selecting the backup function when LSI operation is stopped during switching of the system clock.

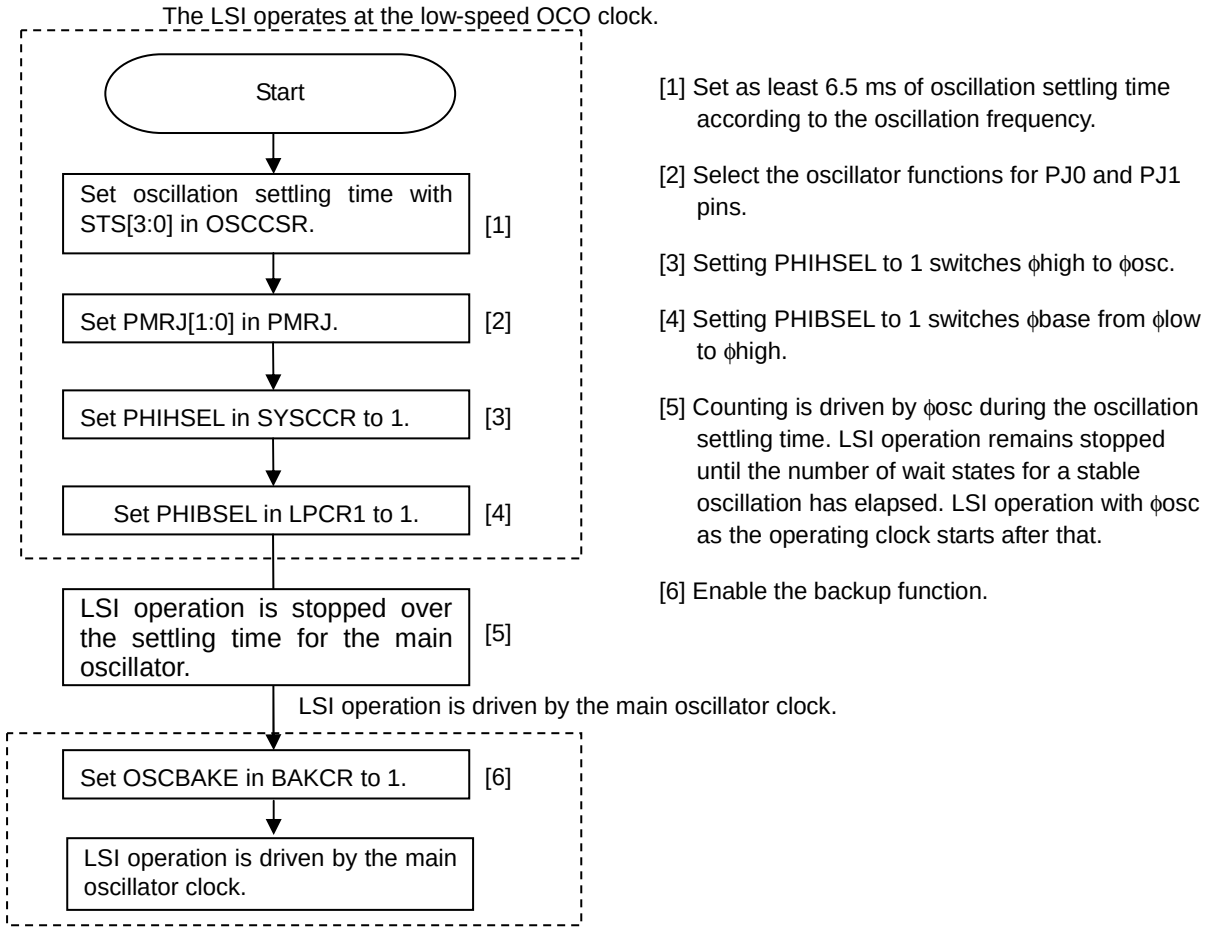

Figure 1 Flowchart of Backup-Function Setting (1)

(2) Figure 2 is a flowchart of the procedure for selecting the backup function when LSI operation is not stopped during switching of the system clock.

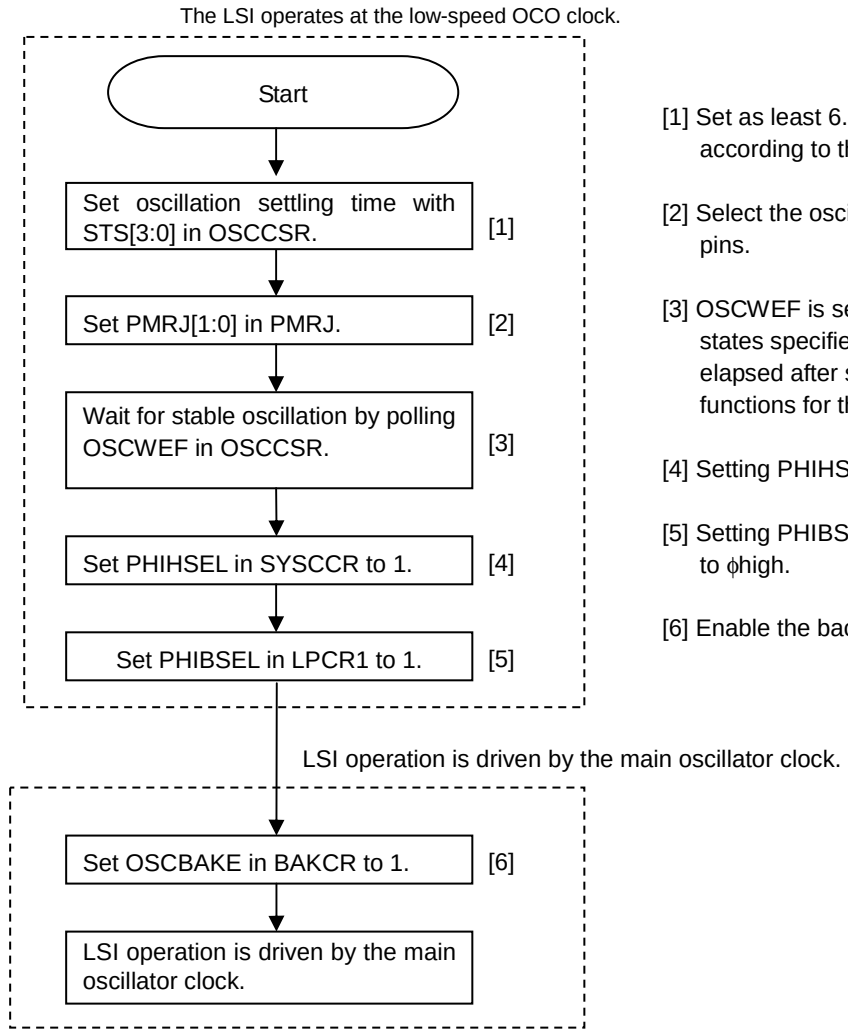

Figure 2 Flowchart of Backup-Function Setting (2)

(3) We are disclosing the function for bit 7 in the OSC oscillation settling control status register (OSCCSR).

Bit	Symbol	Bit Name	Description	R/W
7	OSCWEF	ϕosc oscillation settling wait state completed flag	0: Number of wait states for a stable ϕosc oscillation has not elapsed. 1: Number of wait states for a stable ϕosc oscillation has elapsed. [Setting condition] • The number of states specified by the STS[3:0] bits having elapsed since starting of the main clock oscillator [Clearing conditions] • Switching of the functions of the PJ0 and PJ1 pins from general I/O to the oscillator functions • A transition to standby mode while the PJ0 and PJ1 pins are functioning as oscillator pins • Detection of stoppage of ϕosc oscillation while the backup function is enabled.	R
6 to 4	-	Reserved	These bits are read as 0. The write value should be 0.	-
3 to 0	STS[3:0]	ϕosc oscillation settling time select 3 to 0	Specifies the number of wait states for a stable ϕosc oscillation. For the relationship between assigned values and the numbers of wait states, see table 5.2.	R/W