To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A631A/E	Rev.	1.00
Title	Usage notes of A/D Converter		Information Category	Technical Notification		
Applicable Product	SH7720 Group SH7721 Group SH7705 Group	Lot No. All	Reference Document	SH7720 hardware manual Rev2.00 (REJ09B0033-0200) SH7705 hardware manual Rev2.00 (REJ09B0082-0200)		

There are following usage notes of A/D Converter in the SH7720 Group, the SH7721 Group and the SH7705 Group.

1. There are the amendments of register states in each operating mode of A/D converter in the SH7720 hardware manual (Rev2.00).

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Amendment

Register Abbreviation	Module Standby	
	Original:	Amended:
ADDRA	Retained	Initialized
ADDRB	Retained	Initialized
ADDRC	Retained	Initialized
ADDRD	Retained	Initialized
ADCSR	Retained	Initialized

2. Notes on Clearing the ADF Bit in the ADCSR Register.

Problem: Even though the ADCSR.ADF bit has been read as 1 and 0 was then written to the ADF bit, the ADF bit has not been cleared to 0.

Condition: This problem arises when reading of the ADF bit coincides with setting of the bit to 1 upon the end of A/D conversion.

Avoiding the Problem: Follow any of procedures (a), (b), or (c) below.

(a) Ensure that setting of the ADF bit to 1 upon the end of A/D conversion does not coincide with reading of the ADF bit. For example, read the ADF bit as 1 and then write 0 to the bit during processing of the A/D conversion end interrupt (ADI) that is generated at the end of A/D conversion (when the ADF is set to 1).

(b) If the ADF bit has not been cleared, repeat the operation of reading it as 1 and then writing 0 to it.

(c) Initialize the ADC and clear the ADF bit by placing the ADC in the module standby state.

3. Notes on A/D Conversion in Scan Mode

Problem: A/D conversion in scan mode is not stopped by clearing the ADCSR.ADST bit (to 0).

Condition: This problem arises when 0 is written to the ADST bit in ADCSR to stop A/D conversion while A/D conversion in scan mode is in progress.

Avoiding the Problem: Place the ADC in module standby state after clearing the ADST bit (to 0). Placing the ADC in the module standby state initializes the ADC and stops A/D conversion. When further A/D conversion is required, restart A/D conversion after releasing the ADC from the module standby state.

4. Notes on Transferring the Result of A/D Conversion by the DMAC

Problem: An incorrect superfluous DMA transfer is included before DMA transfer of the correct result of A/D conversion.

Condition: The problem arises in the following cases. Also see the table below:

(a) In Single/Multi Mode

The problem arises when A/D conversion is started while the setting of the ADCSR.DMASL bit is 1, after having proceeded while the setting of the DMASL bit was 0 and then stopped.

(b) In Scan Mode

The problem arises when A/D conversion is started while the setting of the ADCSR.DMASL bit is 1, after having proceeded and stopped.

Table 27.4 Conditions for the Method of Transferring Results of A/D Conversion and Inclusion of Superfluous DMA

The Next Conversion / Current Conversion		In Single/Multi Mode		In Scan Mode	
		DMASL = 0	DMASL = 1	DMASL = 0	DMASL = 1
Single Mode/ Multi Mode	DMASL = 0	Normal	Faulty	Normal	Faulty
	DMASL = 1	Normal	Normal	Normal	Normal
Scan Mode	DMASL = 0	Normal	Faulty	Normal	Faulty
	DMASL = 1	Normal	Faulty	Normal	Faulty

Avoiding the Problem: Follow either of procedures (a) or (b) below.

(a) After A/D conversion has stopped, initialize the ADC by placing it in the module standby state. Start the next round of A/D conversion after releasing the ADC from the module standby state.

(b) Operation under the following conditions ensures that the problem will not arise.

- In Single/Multi Mode

  Transfer when DMASL = 0 → Transfer when DMASL = 0

  Transfer when DMASL = 1 → Transfer when DMASL = 1

- In Scan Mode

  Transfer when DMASL = 0 → Transfer when DMASL = 0