We would like to inform you of the notice about Serial Sound Interface included in the above-mentioned applicable product.

[Notice]
Transmit operation may not be started, even though the TEN bit in Control register (SSICR) is set to 1.

[Workaround]
To start transmit operation, please follow the procedure in figure 1 or figure 2 below.

Figure 1  Transmission Using Direct Memory Access Controller
For \( n = ((\text{CHNL} + 1) \times 2) \)  

**Loop**  

Next channel  

Start  

Release from reset, set SSICR configuration bits.  

Enable transmit operation, enable a data interrupt, enable an error interrupt.  

Wait for more than 1.5 cycles of SSWS.  

IDST = 1?  

No  

Yes  

Disable transmit operation. (\( \text{TEN} = 0 \))  

Wait for more than one cycle of SSSCK.  

Enable transmit operation again. (\( \text{TEN} = 1 \))  

For \( n = ((\text{CHNL} + 1) \times 2) \)  

Loop  

Wait for an interrupt.  

Data interrupt?  

Yes  

No  

Use SSI status register bits to realign data after underflow/overflow.  

Load data of channel \( n \).  

More data to be sent?  

Yes  

No  

Wait for an idle interrupt from this module.  

Release from reset, set SSICR configuration bits.  

Enable transmit operation, enable a data interrupt, enable an error interrupt.  

Wait for more than 1.5 cycles of SSWS.  

IDST = 1?  

No  

Yes  

Disable transmit operation. (\( \text{TEN} = 0 \))  

Wait for more than one cycle of SSSCK.  

Enable transmit operation again. (\( \text{TEN} = 1 \))  

Wait for more than 1.5 cycles of SSWS.  

IDST = 1?  

No  

Yes  

TEN = 1, \( \text{TUIEN} = 1, \text{TOIEN} = 1, \text{TIE} = 1 \)  

Figure 2 Transmission Using Interrupt-Driven Data Flow Control