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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0068A/E	Rev.	1.00
Title	Usage Note for External Bus Controller for DDR3-SDRAM(DBSC3) of RZ/G Series		Information Category	Technical Notification		
Applicable Product	RZ/G Series RZ/G1H, RZ/G1M	Lot No. All lots	Reference Document	RZ/G Series User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

This technical update describes usage note for RZ/G Series.

[Summary]

Usage note for External Bus Controller for DDR3-SDRAM. (RZ/G1H only supports DDR3-SDRAM. RZ/G1M only supports DDR3L-SDRAM.)

[Products]

RZ/G1H, RZ/G1M

[Note]

Add new PHY setting in order to obtain further margin.

This technical update is a revised edition of TN-RZ*-A0058A/E.

[Description]

Add the following description after (c) PHY Setting 1(page15-74), Section 15.4.3.1

The underlined part and bold part are an additional part (change point) of the procedure.

When you change DRAM or your design, change to new setting "(c-2) PHY Setting 1".

Use the following (c-2) PHY Setting 1 in the substitute of (c) PHY Setting 1 in order to obtain further margin.

(c-2) PHY Setting 1

DBSC3_0 Setting:

1. Read the DBDFISTAT register and confirm that 1 is read from INITCOMPL (bit 0).
   When 1 is read, the RESET# pin goes low.
2. Write H'00000011 to the DBDFICNT register.
   This sets the clock frequency ratio and dfi_init_start.
3. Write H'00000003 to the PHY unit address register (DBPDRGA).
4. Write H'0300C4E1 to the PHY unit access register (DBPDRGD) (For DDR3).
   Write H'0300C561 to the PHY unit access register (DBPDRGD) (For DDR3L).
   Set IOM[2:1] of each buffer IO-Mode to the value for DDR3/DDR3L.
5. Write H'00000023 to the PHY unit address register (DBPDRGA).
6. Write H'00FCDB60 to the PHY unit access register (DBPDRGD).

PHY Configuration Setting (Modify according to the memory connected to DDR.)

[17:0]: tREFPRD (9 × tREFI = 9 × 7.8 µs, H'0DB60 at 1600 MHz)

[18]: NOBUB (fixed to 1)

[19]: FXDLAT (fixed to 1)

[27:20]: PUBMODE (fixed to H'0F)

[31:28]: Reserved (must be H'0 since these bits are not used)

7. Write H'00000011 to the PHY unit address register (DBPDRGA).
8. Write H'1000040B to the PHY unit access register (DBPDRGD).
9. Write H'00000012 to the PHY unit address register (DBPDRGA).
10. Write H'9D5CBB66 to the PHY unit access register (DBPDRGD).

DRAM Timing Parameters Setting (Modify according to the memory connected to DDR)

[3:0]: tRTP (DDR3-1600 = H'6 (number of cycles equal to 7.5 ns or more))

[7:4]: tWTR (DDR3-1600 = H'6 (number of cycles equal to 7.5 ns or more))

[11:8]: tRP (DDR3-1600 = H'B (number of cycles equal to 13.75 ns or more (CL = 11)))

[15:12]: tRCD (DDR3-1600 = H'B (number of cycles equal to 13.75 ns or more (CL = 11)))

[21:16]: tRAS (DDR3-1600 = H'1C (number of cycles equal to 35 ns or more (CL = 11)))

[25:22]: tRRD (DDR3-1600 = H'5 (number of cycles equal to 6 ns or more (1-KB page size)))

[31:26]: tRC (DDR3-1600 = H'27 (number of cycles equal to 48.75 ns or more (CL = 11)))

11. Write H'00000013 to the PHY unit address register (DBPDRGA).
12. Write H'1A868300 to the PHY unit access register (DBPDRGD).

DRAM Timing Parameters Setting (Modify according to the memory connected to DDR.)

[1:0]: tMRD (For DDR3, enter the number of cycles to be added to the MIN value, that is 4 cycles. The set value is B'00 for using the MIN condition without additional cycles.)

[4:2]: tMOD (For DDR3-1600, the set value should be 12 cycles equal to 15 ns or more. When the set value is H'0, 12 cycles is specified; as the set value increases by one, the number of cycles increases by one up to 5 cycles.)

[10:5]: tFAW (DDR3-1600 = H'18 (number of cycles equal to 30 ns or more (1-KB page size))

[19:11]: tRFC (The set value is H'0D0 since the cycle is 260 ns for 4 GB.)

[25:20]: tWLMRD (Minimum delay from when write leveling mode is programmed to the first DQS/DQS# rising edge, Default = H'28.)

[29:26]: tWLO (Number of clock cycles from when write leveling DQS is driven high by the control block to when the results from the SDRAM on DQ is sampled by the control block, the set value is H'6 since the DDR3-1600 MAX value is 6.)

[31:30]: tAOND/tAOFD (Default = B'00 since this is only for DDR2.)

13. Write H'00000014 to the PHY unit address register (DBPDRGA).
14. Write H'300214D8 to the PHY unit access register (DBPDRGD).

DRAM Timing Parameters Setting (Modify according to the memory connected to DDR.)

[9:0]: tXS (Self refresh exit delay 5CK to 310 ns: H'005 to H'0F8)

[14:10]: tXP (Power down exit delay 3CK to 6 ns: H'03 to H'05)

[18:15]: tCKE (CKE minimum pulse width 3CK to 5 ns: H'3 to H'5)

[28:19]: tDLLK (DLL locking time 512CK: H'200)

[29]: tRTODT (Read to ODT delay: 1)

[30]: Fixed to 0

[31]: Fixed to 0

15. Write H'00000015 to the PHY unit address register (DBPDRGA).
16. Write H'00000D70 to the PHY unit access register (DBPDRGD).

SDRAM Mode Register 0 Setting (Modify according to the memory connected to DDR.)

[15:0]: set MR0 values.

[31:16]: Reserved (must be 0 since these bits are not used)

17. Write H'00000016 to the PHY unit address register (DBPDRGA).
18. Write H'00000006 to the PHY unit access register (DBPDRGD).

SDRAM Mode Register 1 Setting (Modify according to the memory connected to DDR.)

[15:0]: set MR1 values.

[31:16]: Reserved (must be 0 since these bits are not used)

19. Write H'00000017 to the PHY unit address register (DBPDRGA).
20. Write H'00000018 to the PHY unit access register (DBPDRGD).

SDRAM Mode Register 2 Setting (Modify according to the memory connected to DDR.)

[15:0]: set MR2 values.

[31:16]: Reserved (must be 0 since these bits are not used)

21. Write H'0000001A to the PHY unit address register (DBPDRGA).
22. Write **H'91003DC7 or H'91003DF7** to the PHY unit access register (DBPDRGD).

Set the above values in DATA Training Configuration setting of DDR-PHY.

23. Write H'00000004 to the PHY unit address register (DBPDRGA).
24. Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.

25. **Write H'00000073 to the PHY unit address register (DBPDRGA).**
26. **Write H'14514514 to the PHY unit access register (DBPDRGD).**
27. **Write H'00000074 to the PHY unit address register (DBPDRGA).**
28. **Write H'14514514 to the PHY unit access register (DBPDRGD).**
29. **Write H'00000075 to the PHY unit address register (DBPDRGA).**
30. **Write H'00000514 to the PHY unit access register (DBPDRGD).**
31. **Write H'00000083 to the PHY unit address register (DBPDRGA).**
32. **Write H'14514514 to the PHY unit access register (DBPDRGD).**
33. **Write H'00000084 to the PHY unit address register (DBPDRGA).**
34. **Write H'14514514 to the PHY unit access register (DBPDRGD).**
35. **Write H'00000085 to the PHY unit address register (DBPDRGA).**
36. **Write H'00000514 to the PHY unit access register (DBPDRGD).**
37. **Write H'00000093 to the PHY unit address register (DBPDRGA).**
38. **Write H'14514514 to the PHY unit access register (DBPDRGD).**
39. **Write H'00000094 to the PHY unit address register (DBPDRGA).**
40. **Write H'14514514 to the PHY unit access register (DBPDRGD).**
41. **Write H'00000095 to the PHY unit address register (DBPDRGA).**
42. **Write H'00000514 to the PHY unit access register (DBPDRGD).**
43. **Write H'000000A3 to the PHY unit address register (DBPDRGA).**
44. **Write H'14514514 to the PHY unit access register (DBPDRGD).**

45. **Write H'000000A4 to the PHY unit address register (DBPDRGA).**
46. **Write H'14514514 to the PHY unit access register (DBPDRGD).**
47. **Write H'000000A5 to the PHY unit address register (DBPDRGA).**
48. **Write H'00000514 to the PHY unit access register (DBPDRGD).**

49. Write H'00000001 to the PHY unit address register (DBPDRGA).
50. Write H'00000181 to the PHY unit access register (DBPDRGD).
51. Write H'11000000 to the manual command-issuing register (DBCMD).
52. Write H'00000004 to the PHY unit address register (DBPDRGA).
53. Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.
54. Write H'00000001 to the PHY unit address register (DBPDRGA).
55. Write H'0000FE01 to the PHY unit access register (DBPDRGD).

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