Integrated version of restriction notification

This document is a compilation of the restrictions of the corresponding products that have already been reported, and will be utilized in the NEC microcomputer technical document browsing service. All the restrictions as of September 18, 2001 are included.

NEC Microcomputer Technical Information

CP(K), O

μPD780958 Subseries Usage Restrictions		Document No.	SBG-T-2509-E		1/1
		Date issued	September 18, 2001		
		Issued by	Microcomputer Engineering Dept. Solution Engineering Div. NEC Electron Devices NEC Corporation		
Related documents	User's manual (controlled by engineering department) Data sheet (U14590EJ1V1DS00)	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected products

   μPD780956, 780958

   μPD78F0958 (ES)

2. List of restrictions

   The restriction history and detailed information is described in Attachment 1.

List of Restrictions in μPD780958 Subseries

1. Product Version

μPD780956, 780958: Rank K, E
μPD78F0958: Rank K

***** The rank is indicated by the fifth character from the left in the lot number marked on the package.

List of Restrictions

<Mask ROM version>

Description		UPD780956, 780958	
	Rank	K	E
Item 1	Supplement to explanation in manual related to 16-bit timer	Δ	Δ
Item 2	Change of capacitor value for built-in regulator	Δ	Δ
Item 3	Caution on EMS noise tolerance	Δ	Δ
Item 4	Restriction on 16-bit timer	Δ	Δ
Item 5	Bug in MR sampling function	×	√

<Flash memory version>

Description		UPD78F0958
	Rank	K
Item 1	Supplement to explanation in manual related to 16-bit timer	Δ
Item 2	Change of capacitor value for built-in regulator	Δ
Item 3	Caution on EMS noise tolerance	Δ
Item 4	Restriction on 16-bit timer	Δ
Item 5	Bug in MR sampling function	Δ

Notes 1. The rank is indicated by the fifth character from the left in the lot number marked on the package.

2. The meaning of each symbol is as follows.

–: Restriction does not apply
√: Restriction already corrected
×: Restriction applies (correction is planned)
Δ: Restriction applies (correction is not planned)

3. Details of Usage Restriction

Item 1: Refer to Attachment 2 for details.

Item 2: Refer to Attachment 3 for details.

Item 3: Refer to Attachment 4 for details.

Item 4: Refer to Attachment 5 for details.

Item 5: Refer to Attachment 6 for details.

4. Other Cautions

None.

Item 1. Supplement to explanation in manual related to 16-bit timer

[Description]

This report is intended to provide supplementary information for explanations related to 16-bit timer/event counter 2 in the user's manual that were insufficient.

<Overview of operation>

When using 16-bit timer/event counter 2 as an event counter, the first or second clock after operation starts will be invalid.

<Operation details>

The above devices and 16-bit timer/event counter 2 of the ICE operate as follows.

<Operation when using the internal clock as a counter clock>

From when TCE2 is set until the count value is cleared*

→ Counter value of timer 2 = The actual number of clocks input − 1

After the count value is cleared

→ Counter value of timer 2 = The actual number of clocks input

<Operation when using the external clock as a counter clock>

From when TCE2 is set until the count value is cleared*

→ Counter value of timer 2 = The actual number of clocks input − 2

After the count value is cleared

→ Counter value of timer 2 = The actual number of clocks input

*: Until the count value is cleared by matching with the compare register or overflow.

The supplement to the above description is described in Attachments 3 to 5.

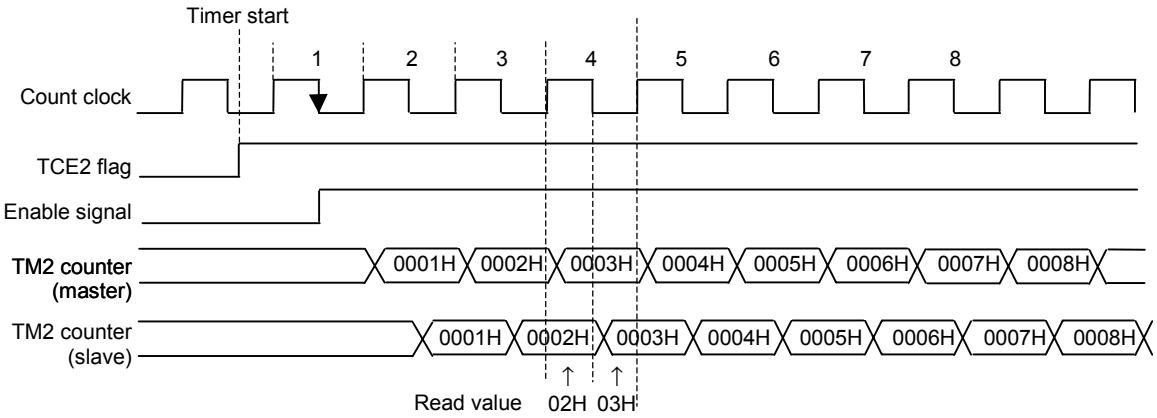
[Workaround]

The description will be modified when the document is next revised.

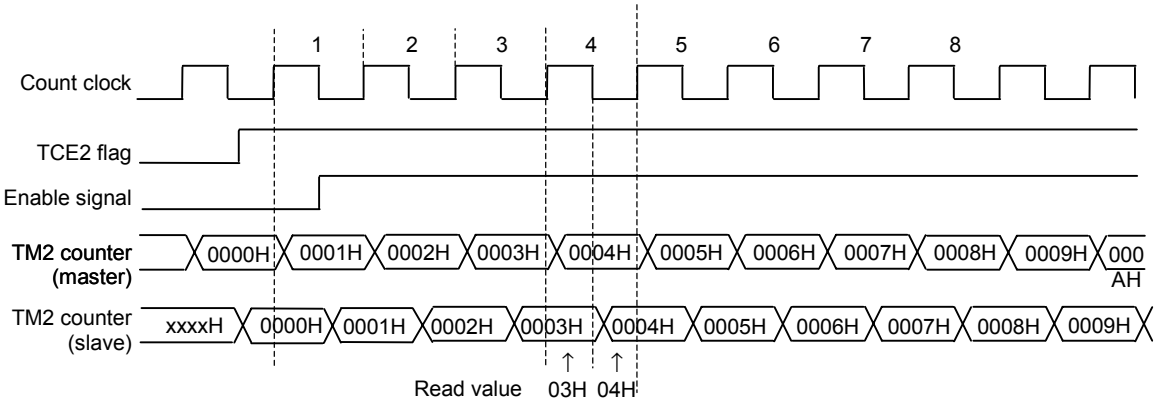
[Internal clock]

<First read value after counter starts (before match and clear)>

* Counter read begins from the TM2 counter (slave).



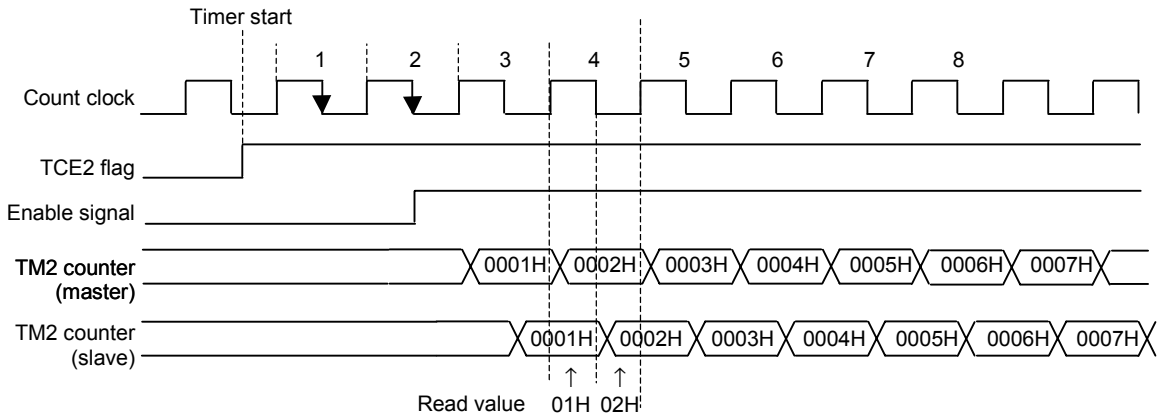
<From second read value after counter starts (after match and clear)>



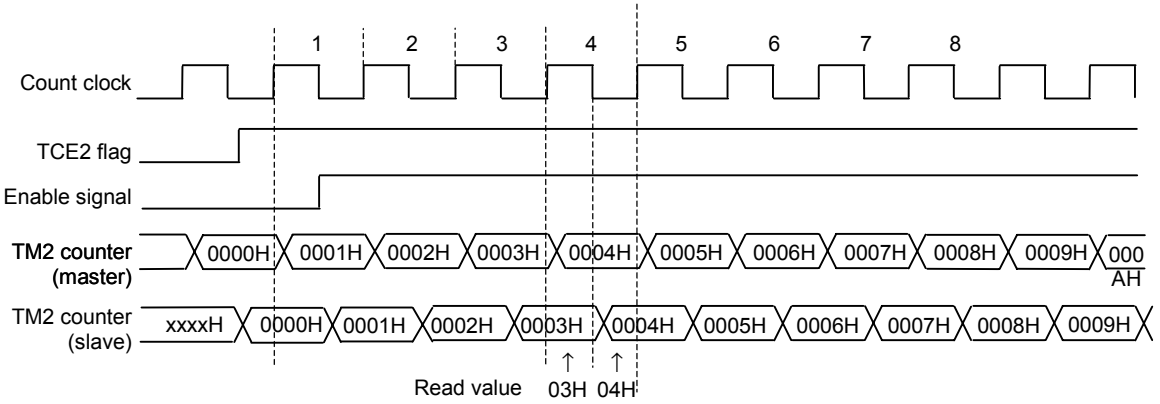
[External clock]

<First read value after counter starts (before match and clear)>

* Counter read begins from the TM2 counter (slave).



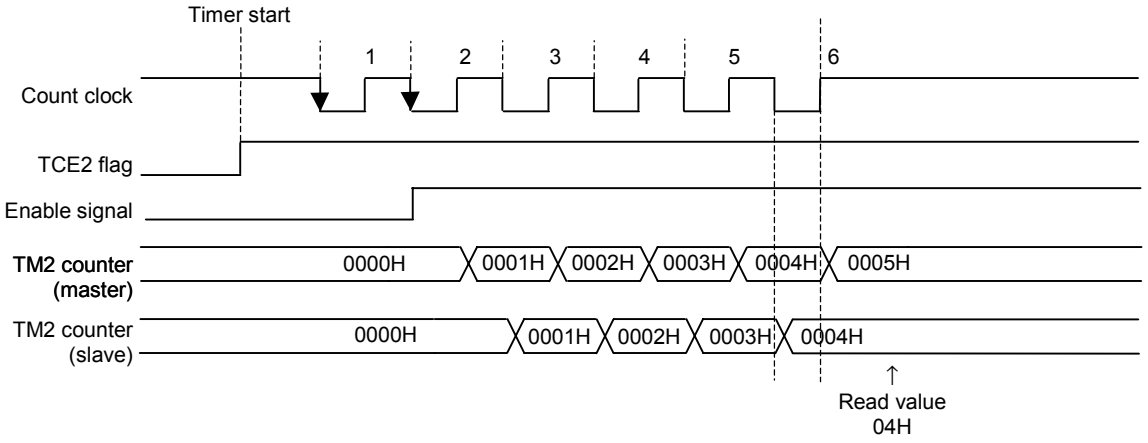
<From second read value after counter starts (after match and clear)>



[Example of using external clock input]

External clock input will be exactly as in the timing diagram below in all cases when used in accordance with the following conditions. Consequently, adding 2 to the count value read is acceptable.

- External event count
- Clock is used at low active
- Start instruction is performed when there is no external event input (high), or when there is no external event input (high) while executing a read instruction after an external event is input.



Item 2. Change of capacitor value for built-in regulator

[Description]

The value of the capacitor that is externally attached to the connection pins VRout0 and VRout1 of the capacitor for the built-in regulator noted in the preliminary user's manual (document number: U13655EJ1V0UM00) has been changed.

Final evaluation by NEC indicated that extremely stable regulator output is possible by setting the capacitor that is attached to the VRout0/VRout1 pin to 10 μF. Therefore, NEC recommends this capacitance value.

Current (as noted in the manual):

0.47 μF

After revision:

10 μF

[Workaround]

The description will be modified when the document is next revised.

Item 3. Caution on EMS noise tolerance

[Description]

One difference between the mask ROM and flash memory products is their internal operating voltage. The mask ROM product has an internal regulator that keeps the CPU operating voltage low in order to reduce the power consumption. The flash memory product does not have this regulator. Be sure to evaluate the mask ROM product thoroughly before use.
The evaluation data on EMI noise tolerance, which requires a particular attention, is reported below.

<Measurement method>

- Noise application

  Noise applied to the power supply line of the target board using noise simulator, while running an NEC evaluation program on the board.

- Evaluation program

  All instructions excluding the HALT and STOP instructions are executed repeatedly while outputting a square wave of a given interval from P01. If an instruction is not executed correctly, or if the result of executing an instruction is not correct, the program stops the output of the square wave.

- Malfunction detection method

  Noise is applied to the board at a specified voltage for one minute, and the voltage value (min.) at which the output pulse stops is measured.

- Noise application period: 1 minute
- Applied pulse characteristics

  Pulse width: 50 ns

  Pulse frequency: 100 Hz
- Number of samples: 3

<Measurement conditions>

- Supply voltage [VDD]: 3.0 V
- Measurement temperature [T_A]: 25°C
- Oscillator frequency [f_X]: 1.2 MHz

  [f_{XT}]: 32.768 kHz
- Clock select register [PCC]: 00H/01H/02H

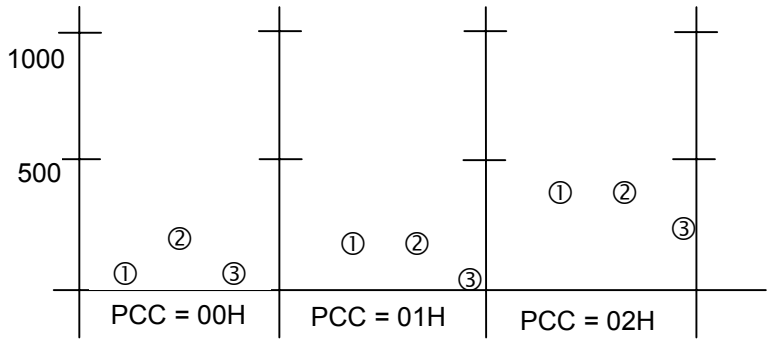
<Measurement environment>

- Evaluation equipment: Noise simulator 1100 (Big Bang)
- Noise application conditions: Applied to both VDD and GND lines

<Results of measuring EMS noise tolerance>

Device: μPD780958(A)

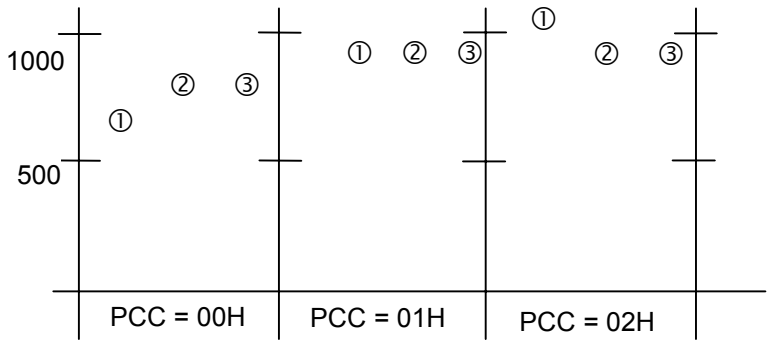
Note: The circled numbers indicate sample numbers. The position of the sample number indicates the maximum voltage at which correct operation was confirmed for the sample.



* The values in this data are presented only as reference values measured with specific samples, and do not imply any guarantee. These values are not guaranteed values.

Device: μPD78F0958

Note: The circled numbers indicate sample numbers. The position of the sample number indicates the maximum voltage at which correct operation was confirmed for the sample.



* The values in this data are presented only as reference values measured with specific samples, and do not imply any guarantee. These values are not guaranteed values.

Item 4. Restriction on 16-bit timer

[Description]

The source of the counter clear and start in the one-shot trigger mode of the 16-bit timer is the AND condition of the software trigger (OSPTn = 1) and the external trigger input (TI input). Selecting only one of them is disabled. (n = 0, 1).

As a result, the output pulse generated by the software trigger generates a trigger again, resulting in the same operation as PPG instead of a one-shot pulse operation.

[Workaround]

Use of the one-shot pulse output mode is prohibited. The description of the one-shot pulse output mode will be deleted from the user's manual.

Item 5. Bug in MR sampling function

[Description]

When the MR sampling output mode of the MR sampling function is used, unexpected clocks are output.

<Example> Setting: TCM0 = 91H, TMM0 = 00H, MRM0 = 01H

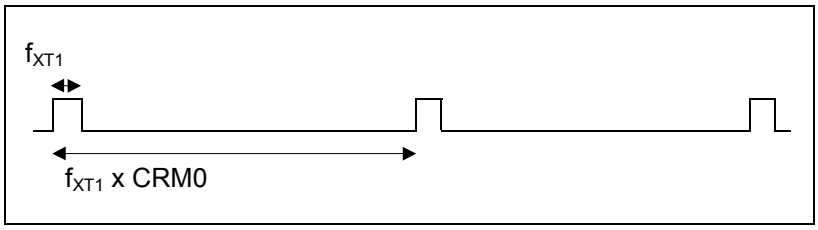


Figure) Normal Waveform

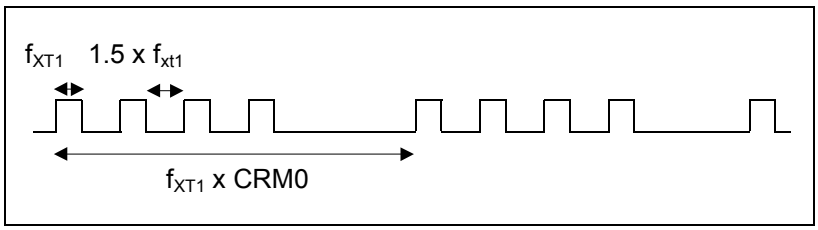


Figure) Bug Waveform

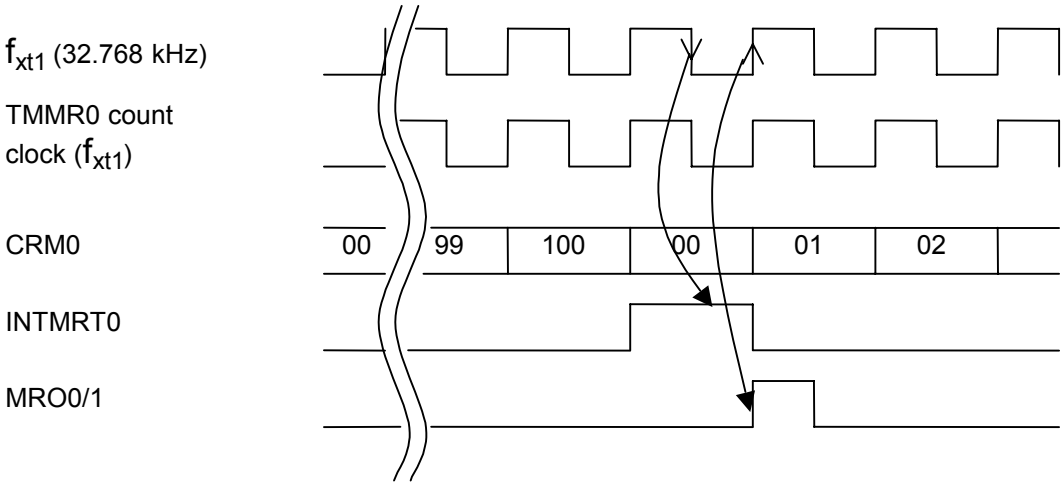
<Cause>

- Normal operation: Count clock width of TMMR0 < Output clock pulse width of MR00/1

This device monitors the level of the interrupt request signal (INTMRT0) at the fall of f_{XT1} (f_{XT2}). When it recognizes the high level of INTMRT0, it outputs one pulse from MR00/1 at the next rise of f_{XT1} (f_{XT2}). Here, INTMRT0 retains “HI” for 1 clock width of the TMMR count clock.

(Operation example)

Condition: Count clock of TMMR0 = f_{XT1} (30.5 μs)
Output clock pulse width of MR00/1 = 2 x f_{XT1} (15 μs)
Compare register (CRM0) = 100

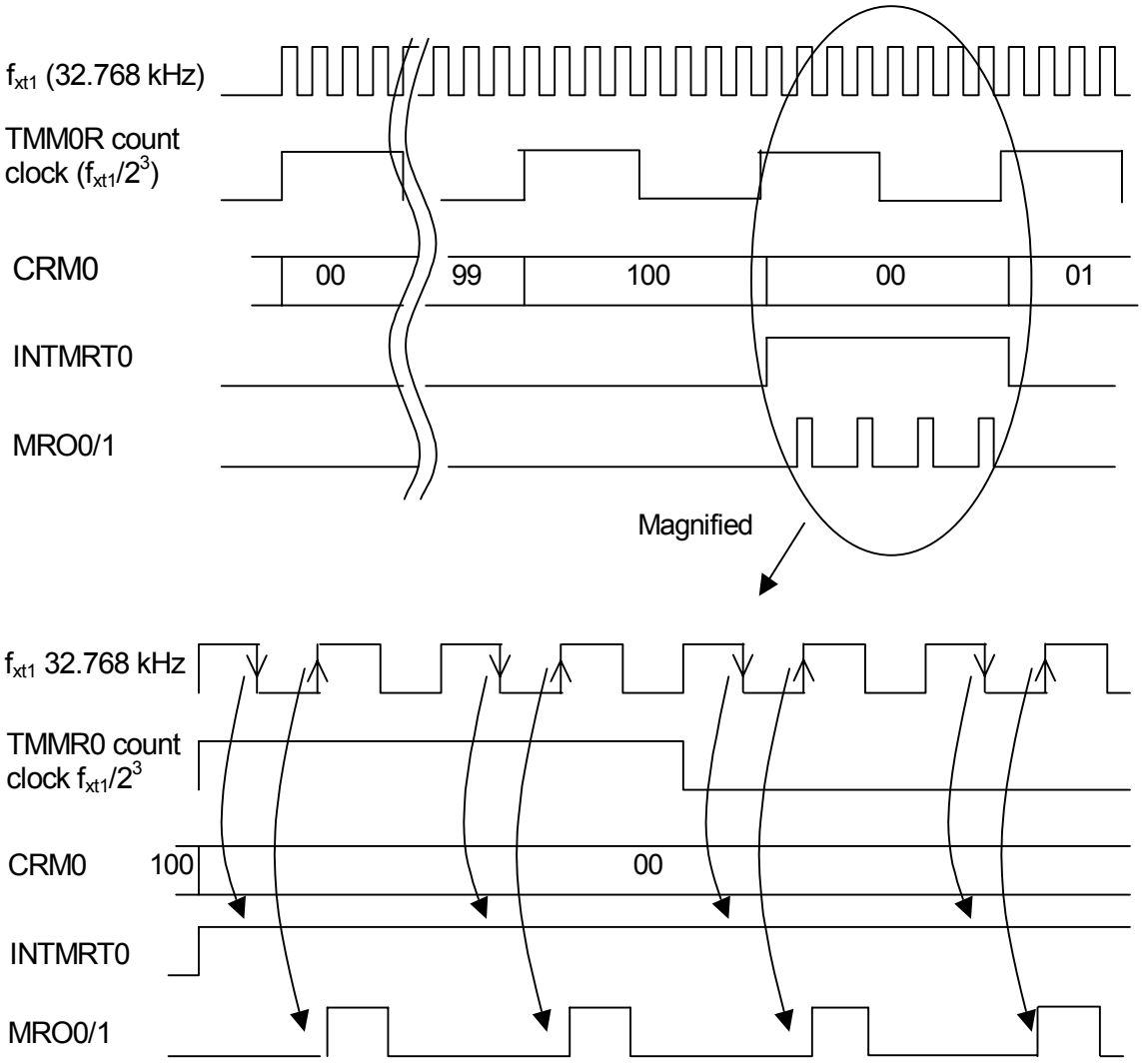


- Abnormal operation: Count clock width of TMMR0 > Output clock pulse width of MR00/1

  When this device recognizes the "HI" level of INTMRT0 at the fall of f_{XT1} (f_{XT2}), it outputs one pulse from MR00/1 at the next rise of f_{XT1} (f_{XT2}). Likewise, it outputs one pulse from MR00/1 at the next rise of f_{XT1} (f_{XT2}) when INTMRT0 is in the "HI" state. Therefore, as long as INTMRT0 is in the "HI" state, pulses are continuously output from MR00/1.

- Setting example

  Condition: Count clock of TMMR0 = f_{XT1}/23 (244 μs)
  Output clock pulse width of MR00/1 = 2 x f_{XT1} (15 μs)
  Compare register (CRM0) = 100


f_{xt1} (32.768 kHz)
TMM0R count clock ($f_{xt1}/2^3$)
CRM0
00
99
100
00
01
INTMRT0
MRO0/1
Magnified
f_{xt1} 32.768 kHz
TMMR0 count clock $f_{xt1}/2^3$
CRM0
100
00
INTMRT0
MRO0/1

[Workaround]

<Temporary workaround>

MR sampling is performed in accordance with the settings in the table below.

Devise a countermeasure using software referring to these settings.

TMMR Count Clock			Output Clock Pulse Width Setting of Selectable MR01/MR00 Pin			
			CK01=0/CK00=0	CK01=0/CK00=1	CK01=1/CK00=0	CK01=1/CK00=1
TCM01	TCM00	f_{XT1}	2 x f_{XT1}	f_{XT1}	$f_{XT1}/2$	$f_{XT1}/2^5$
0	0		√	√	√	√
0	1	$f_{XT1}/2^3$	*	*	*	√
1	0	$f_{XT1}/2^7$	*	*	*	*
1	1	$f_{XT1}/2^4$	√	√	√	√

√: Operates normally.

*: Care must be exercised because unexpected waveforms will be generated.

<Permanent countermeasure>

The hardware will be corrected for mask ROM products.

For development tools, the device files will be corrected.

* Please take note that the μPD78F0958 will not be corrected. We sincerely apologize for the inconvenience this may cause.