NEC Microcomputer Technical Information

CP(K), O

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µPD780228 Subseries Usage Restrictions		Date issued	September 18, 2001	
		Issued by	Microcomputer Engineering Dept. Solution Engineering Div. NEC Electron Devices NEC Corporation	
Related documents	User's manual (controlled by engineering department) Data sheet (U11797EJ1V0DS00)	Notification classification	√	Usage restriction
				Upgrade
				Document modification
				Other notification

1. Affected products
    µPD780226
    µPD780228

2. List of restrictions
    The restriction history and detailed information is described in Attachment 1.

List of Usage Restrictions in μPD780228 Subseries

1. Product Version

μPD780226, 780228: Rank K

* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

2. Product History

<Mask ROM version>

Description		UPD780226 UPD780228
	Rank	K
Item 1	Restriction on VFD display	Δ

Notes 1. The rank is indicated by the fifth character from the left in the lot number marked on the package.

     2. The meaning of each symbol is as follows.

       −: Restriction does not apply

       √: Restriction already corrected

       ×: Restriction applies (correction is planned)

       Δ: Restriction applies (correction is not planned)

3. Details of Usage Restrictions

Item 1: Refer to Attachment 2 for details.

4. Other Cautions
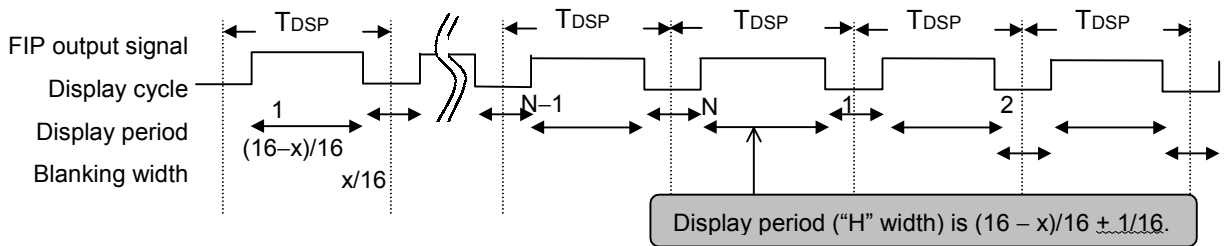
None.

Item 1. Restriction on VFD display

[Description]

The operation varies according to the specifications of the blanking width, number of display pattern, display cycle, key scan cycle insertion as follows.

Blanking Width		1/16	2/16	4/16	6/16	8/16	10/16	12/16	14/16
Key scan cycle	Not inserted	The Nth display period is +1/16. (See <1>.)		The blanking width between "N − 1" and "N" is x/16 + 1/16. (See <2>.)					
	Inserted	The key scan cycle is TDSP + 1/16. (See <3>.)							

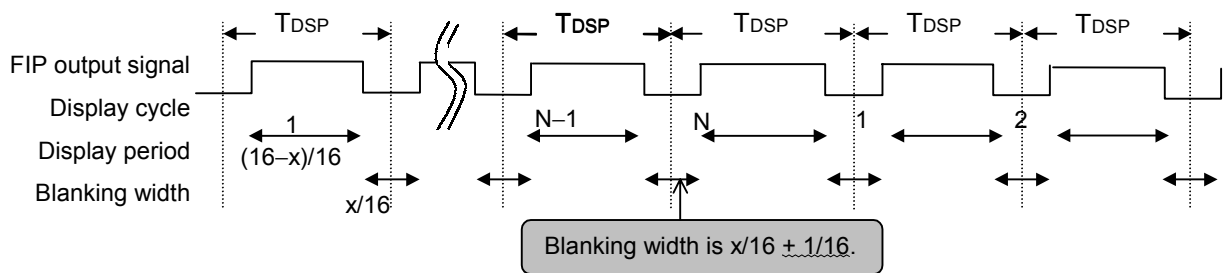**Note** The example of output waveform is shown in <1>, <2>, <3> below.

<1> Condition: Blanking width: 1 or 2, key scan cycle: Not inserted

FIP output signal
Display cycle
Display period
Blanking width

T_{DSP} T_{DSP} T_{DSP} T_{DSP} T_{DSP}

1   N−1   N   1   2
(16−x)/16
x/16

Display period ("H" width) is (16 − x)/16 ± 1/16.

Remarks 1. Display cycle: TDSP = 1 (Normal: 16/16)
2. x = 1, 2, 4, 6, 8, 10, 12, 14 (Set value for DSPM1.5 to DSPM1.7)

<2> Condition: Blanking width: 4 to 16, key scan cycle: Not inserted

FIP output signal
Display cycle
Display period
Blanking width

T_{DSP} T_{DSP} T_{DSP} T_{DSP} T_{DSP}

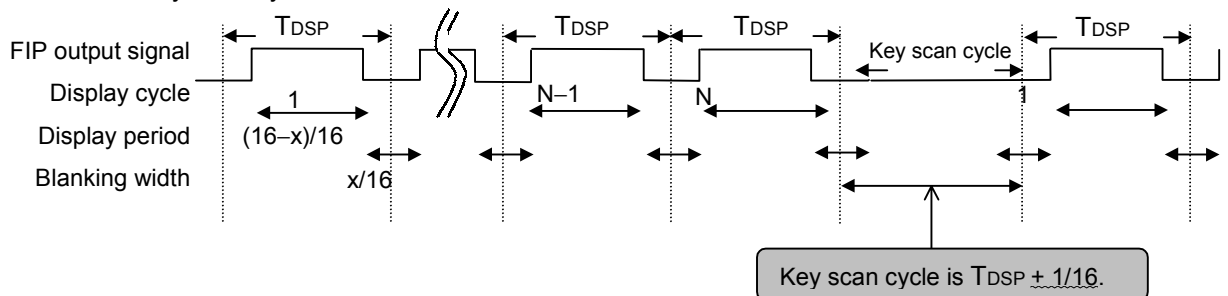1   N−1   N   1   2
(16−x)/16
x/16

Blanking width is x/16 ± 1/16.

Remarks 1. Display cycle: TDSP = 1 (Normal: 16/16)
2. x = 1, 2, 4, 6, 8, 10, 12, 14 (Set value for DSPM1.5 to DSPM1.7)

<3> Condition: Key scan cycle: Not inserted

FIP output signal
Display cycle
Display period
Blanking width

T_{DSP} T_{DSP} T_{DSP} Key scan cycle T_{DSP}

1   N−1   N   1
(16−x)/16
x/16

Key scan cycle is T_{DSP} ± 1/16.

Remarks 1. Display cycle: TDSP = 1 (Normal: 16/16)
2. x = 1, 2, 4, 6, 8, 10, 12, 14 (Set value for DSPM1.5 to DSPM1.7)

[Workaround]

Regard this as a usage restriction. This information will be added when the document is next revised.