To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

MESC TECHNICAL NEWS

No. M7700-46-9906

Notes on Using DMA Controller (DMAC) in 7920 Group MCUs

1. Related Devices

All of the 7920 series MCUs

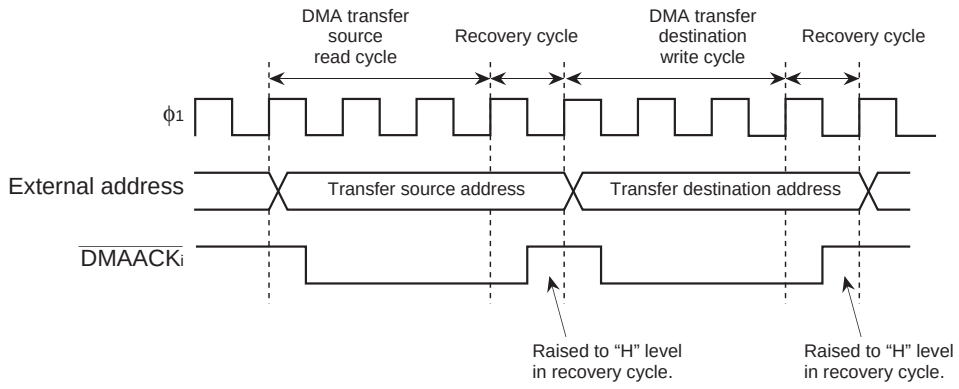
2. Symptom

When the $\overline{\text{DMAACK}}_i$ validity bit for a DMA transfer is set to “valid”, if the following conditions are satisfied, there is a possibility that the active “L” level output from pin $\overline{\text{DMAACK}}_i$ is raised to “H” level. (In a certain period, this “H” level output is retained.);

[Condition 1]
A recovery cycle is inserted to a certain cycle for accessing a transfer source area or a transfer destination area.

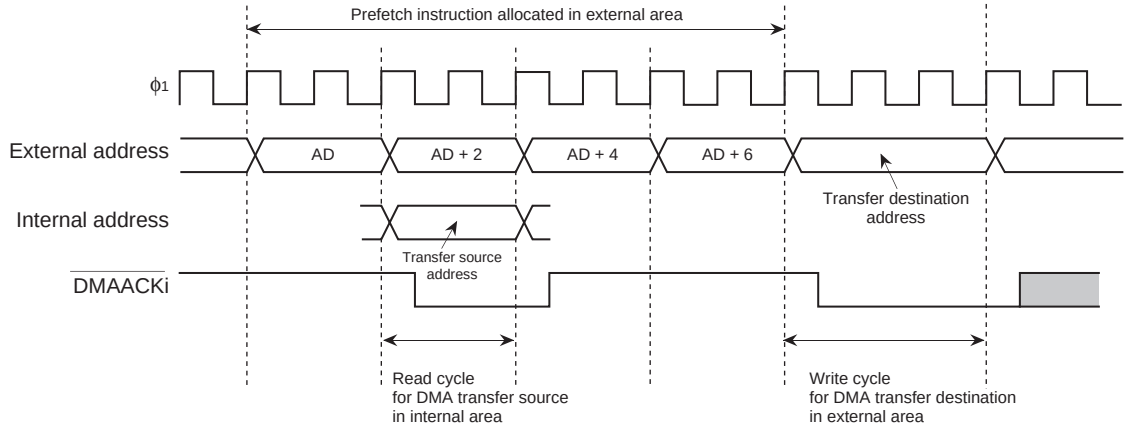
Pin $\overline{\text{DMAACK}}_i$ is raised to “H” level at the falling edge of ϕ_1 in a recovery cycle. When the DMA transfer continues (the burst transfer mode, or 2-bus-cycle transfer in the cycle steal mode), pin $\overline{\text{DMAACK}}_i$ returns to “L” level at the first falling edge of ϕ_1 in the next bus cycle.

Example:



[Condition 2]
In the 2-bus-cycle transfer during prefetch of an instruction allocated in the external area, the internal area is designated for the transfer source, and the external area is designated for the transfer destination, respectively.

Example:



[Condition 3]
A DRAM refresh is executed during a 2-bus-cycle transfer.

Example: