To our customers,

# Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

GRADE A

# MAEC TECHNICAL NEWS

No. M32R-03-0209

## M32R/ECU Series: Note on Using Interrupts

| Classification | Concerned Products |
|---|---|
| Corrections and supplementary explanation of document<br>√ Notes<br>Knowhow<br>Others | M32R/ECU Series |

### [Note]

When all of the following conditions occur at the same time and an interrupt for (A') is generated during the period from "when the IVECT is read out until the interrupt mask register (IMASK) is restored," the interrupt (A') request is processed as an interrupt (A) request at the point it is generated. The request for interrupt (B) is not processed until after interrupt (A) process is completed.

### [Occurrence Conditions]

The following describes the problem and related conditions concerning use of multiple interrupts.

(1) The problem occurs when using "Edge-recognized" interrupt (A) with interrupt (B), which has a higher interrupt priority level than (A), and
(2) when interrupt (B) is generated between the time the handler process for interrupt (A) has started and the interrupt vector register (IVECT) has been read out, and
(3) when multiple interrupts are not enabled (immediately after reading out the IVECT in the interrupt handler, the IE bit of PSW is not set to "1" and multiple interrupts are not enabled), and
(4) when a second request for interrupt (A) is generated within the interrupt (A) process. (The second request for interrupt (A) will be referred to as "interrupt (A') request" in this document.)

The following two sections describe this note in detail.

## [Operations under Normal Conditions]

Figure 1 shows interrupt handler processing under normal operating conditions.

Under normal operating conditions, the “Edge-recognized” interrupt request is cleared when the interrupt vector register (IVECT) is read out in the interrupt handler process. After the request is cleared, the next interrupt request can be detected.

Therefore, under normal operating conditions, if an interrupt request for (A’) is generated during the period from “when an interrupt (A) request is generated until the interrupt request is cleared after the IVECT is read out,” the interrupt (A’) request is processed as an interrupt (A) request at the point it is generated, and if a request for interrupt (A’) is generated after the current (A) interrupt request is cleared, it will be processed as an interrupt (A’) after the interrupt (A) process is completed.

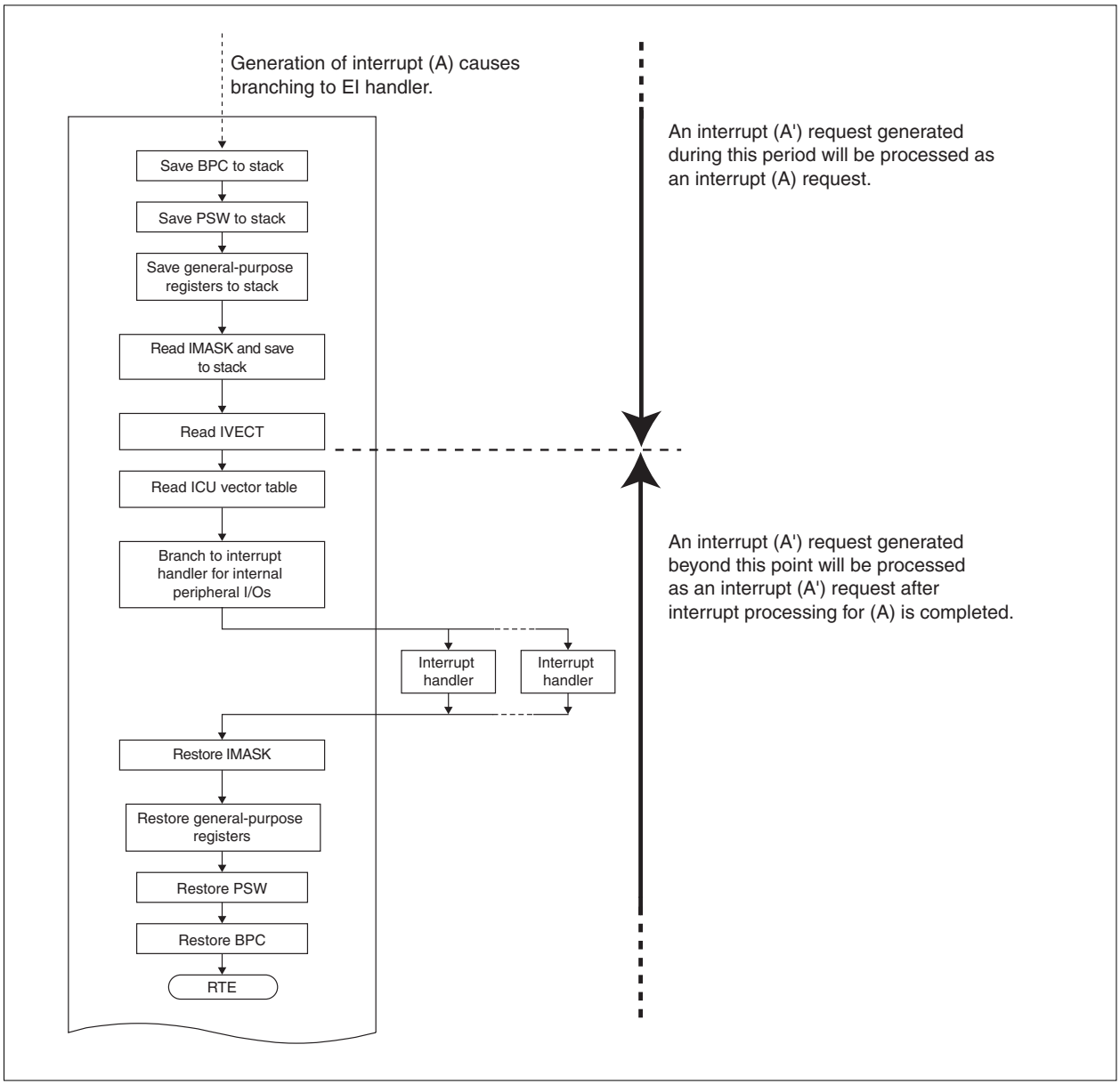


Figure 1. Interrupt Handler Process under Normal Operating Conditions

## [Operations Under which Current Problem Occurs]

Figure 2 shows the operations for interrupt handler processing in which the current problem occurs.

When conditions 1 through 4, listed previously, occur at the same time, the interrupt request clear signal (internal signal) for either (A) or (A') is continually output during the period from "when the interrupt vector register (IVECT) is read out until the interrupt mask register (IMASK) is restored". Therefore, an interrupt request for (A') that occurs during the period from "when IVECT is read out until IMASK is restored" is processed as an interrupt (A) request within the current interrupt processing.

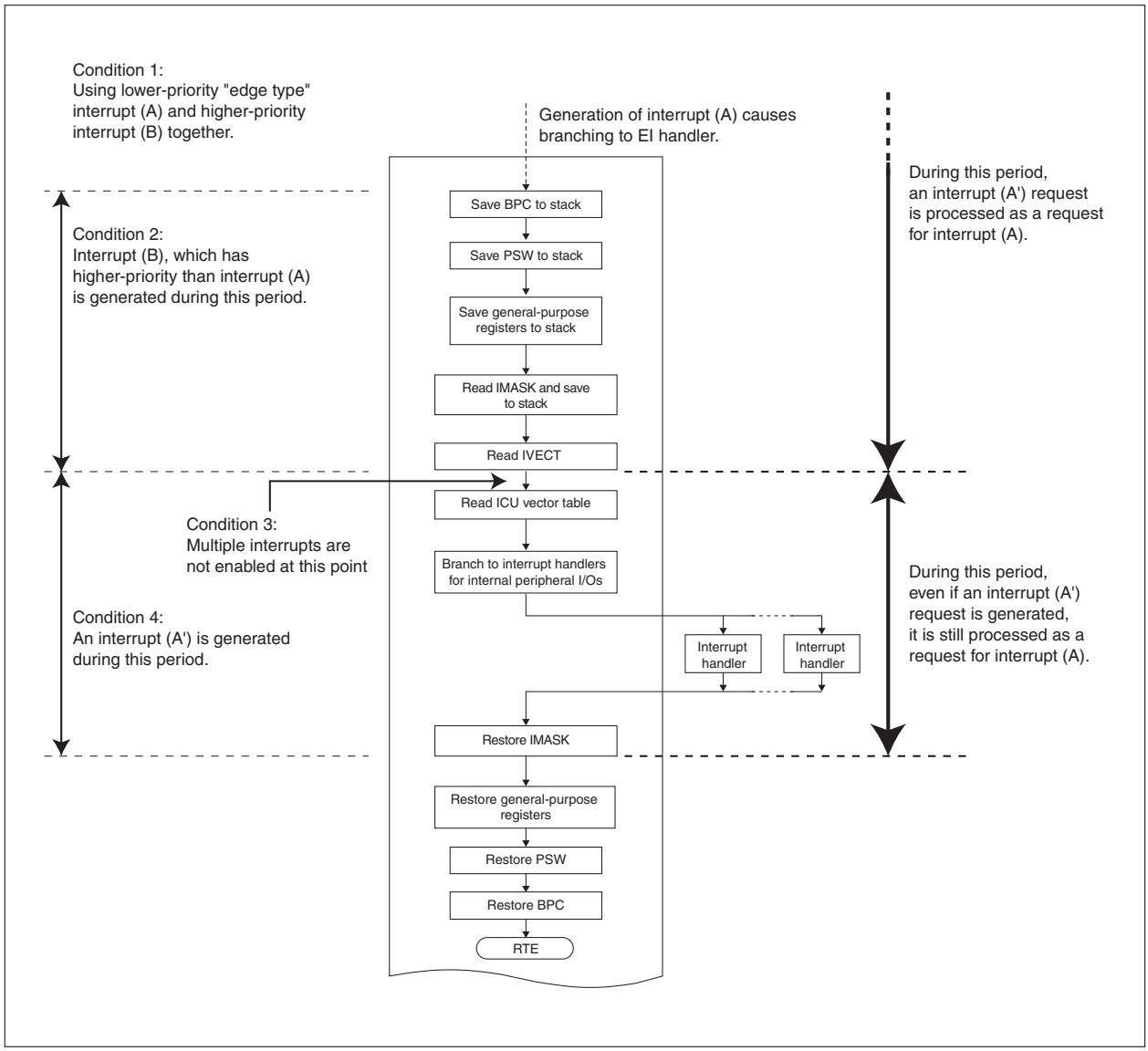


Figure 2. Interrupt Handler Operations when Current Problem Occurs.

[Countermeasure]

As shown in Figure 3, immediately after the interrupt vector register (IVECT) is read out during the interrupt handler, add an instruction to overwrite the current interrupt mask register (IMASK) value in the IMASK.

By adding this instruction, the continuous output of the interrupt request clear signal for (A) or (A') will be cancelled, enabling detection of an interrupt request for (A') during the period from "when the IMASK is overwritten until the IMASK is restored".

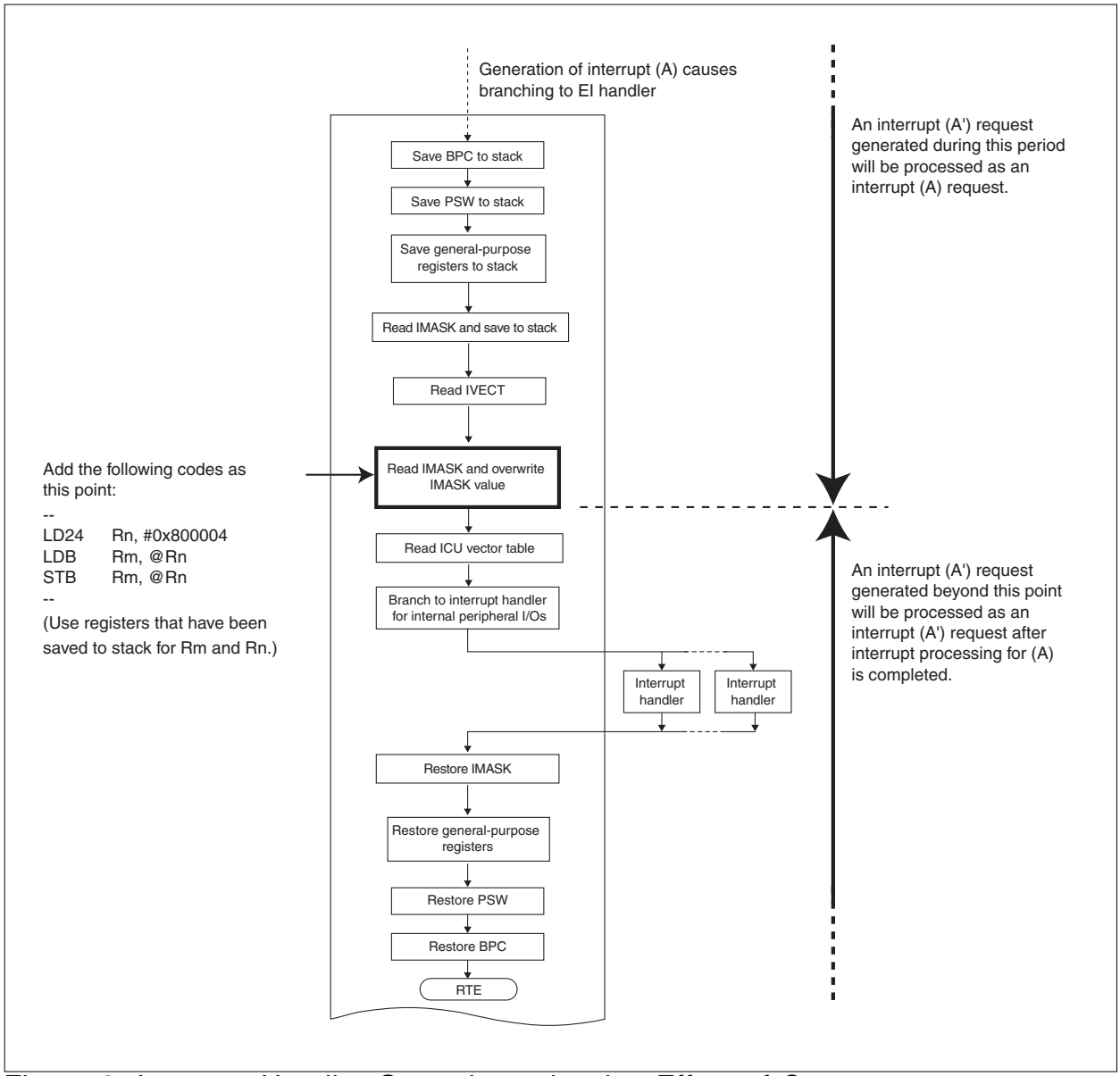


Figure 3. Interrupt Handler Operations showing Effect of Countermeasure