To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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GRADE A

RENESAS TECHNICAL NEWS

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3874 Group
Usage Notes for Clearing Multiple Factors/One Vector Interrupt Request Bit

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	3874 Group

When setting the interrupt request bit for multiple factors/one vector interrupt to 0 , set the request bit of the interrupt source discrimination register to 0 before setting 0 to the interrupt request bit for multiple factors/one vector interrupt , or set the interrupt request bit for multiple factors/one vector interrupt to 0 in the state of the interrupt disable flag (I) = 1 .

[Reason]

If setting the interrupt request bit for multiple factors/one vector interrupt to 0 before setting the request bit of the interrupt source discrimination register to 0 , the interrupt request bit for multiple factors/one vector interrupt may not be set to 0 by other interrupts occurrence.

Example 1

```
        :
LDM   #00h, IREQD1   ; INT3 interrupt request bit to 0 setting
                     ; (Request bit of interrupt source discrimination register to 0 setting)
LDM   #00h, IREQ2    ; INT3, INT4, INT5 interrupt request bit to 0 setting
        :            ; (Interrupt request bit for multiple factors/one vector interrupt to 0 setting)
```

Example 2

```
        :
SEI                  ; All interrupts disabled
LDM   #00h, IREQ2    ; INT3, INT4, INT5 interrupt request bit to 0 setting
                     ; (Interrupt request bit for multiple factors/one vector interrupt to 0 setting)
LDM   #00h, IREQD1   ; INT3 interrupt request bit to 0 setting
        :            ; (Request bit of interrupt source discrimination register to 0 setting)

CLI                  ; Interrupts enabled
        :
```

Note: IREQD1= Interrupt source discrimination register 1 (address 0038_{16})
IREQ2= Interrupt request register 2 (address $003D_{16}$)