

# RENESAS TECHNICAL UPDATE

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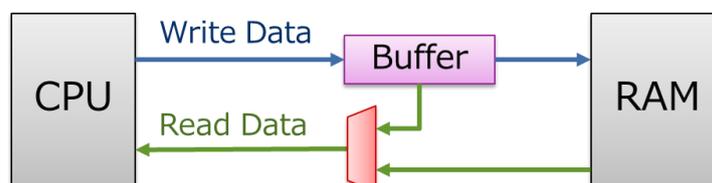
Product Category	MPU/MCU		Document No.	TN-SH7-A912A/E	Rev.	1.00
Title	Supplementary explanation on RAM self-test		Information Category	Technical Notification		
Applicable Product	SH7147 Series	Lot No.	Reference Document	SH7147 Group Hardware Manual Rev.3.00 (REJ09B0230-0300)		
		All lots				

This is a supplementary explanation for customers who perform RAM self-tests to achieve functional safety or for any other purposes while a MCU is operating.

## <Supplementary explanation>

With the above-mentioned applicable products, a buffer for high speed access is allocated between RAM and a CPU as illustrated below. When a value is written to RAM and then execute a read access to the same address, the value may be read from the buffer, not from the RAM.

The structure having a buffer will not functionally affect write/read operation. However, with a program in which a written value is to be read from RAM, the assumed (expected) operation may not be achieved. (In some cases, the written value is read from a buffer.)



Perform the following operation to ensure that a value will be read from RAM.

To read RAM data at an address of 4-aligned bytes (\*) after writing a value to the RAM address of the same 4-aligned bytes:

Write a value to any other RAM address which is out of the 4-aligned bytes, and then execute a read access to the RAM address where you want to read.

(\*) With 4-aligne bytes, the lower two bits of the address are a range of 00b to 11b.

Example) When the access range is within 0400h through 0403h, access a RAM address within this range first and then access a RAM address outside this range.

Note that values read from a buffer and RAM are the same even if the value is read from the buffer, not from the RAM. Thus, the behavior of your program will not be affected even if this supplementary note is ignored.

However, please be aware that this (an unintentional read operation from a buffer) may happen when a value needs to be read directly from RAM (e.g. when performing a self-test for an internal RAM).