

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	LCD driver	Document No.	TN-PLC-A006A/E	Rev.	1.00
Title	Supplementary explanation on deep-standby_R61505U, R61505		Information Category	Technical Notification	
Applicable Product	R61505U, R61505	Lot No.	Reference Document		
		All			

This letter provides supplementary explanation and instruction on deep-standby function.

Our datasheets state that “Low” CS signals must be inputted six times in order to cancel deep-standby mode. However they do not provide enough information on other interface control signals. This letter is to add explanation on how to deal with them.

LSI's operation is not defined until finishing inputting CS signals six times. In order to avoid write operation by WR signal and read operation by RD signal during this period, we ask for your system(s) to be designed so that WR and RD signals are set at “High” level. RS signal may be either “High” or “Low” because it is selection signal of index register and write-in data.

Data signals may be either any data input status or HiZ status.

When canceling deep-standby mode by inputting CS signals six times writing data at the same time, it is possible that index register is accessed resulting in undesirable write-in operation and then LSI's malfunction.

If your system design makes it difficult to input CS signal independently (for example, inputting WR signal synchronized with CS signal), please make sure to follow charts below in canceling deep-standby mode.

Instruction on deep-standby cancellation setting (When the system do not allow independent CS “Low” signal

input)

(1) 16-/18- bit interface mode

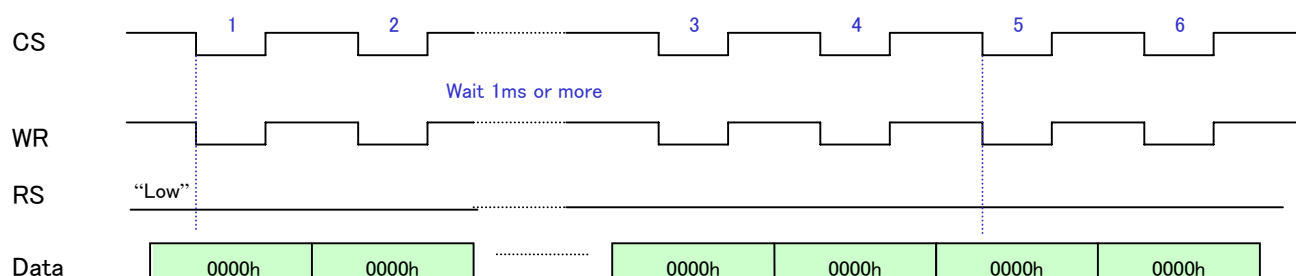


Figure 1 Signal input timings when canceling deep-standby mode (16 bit interface mode)

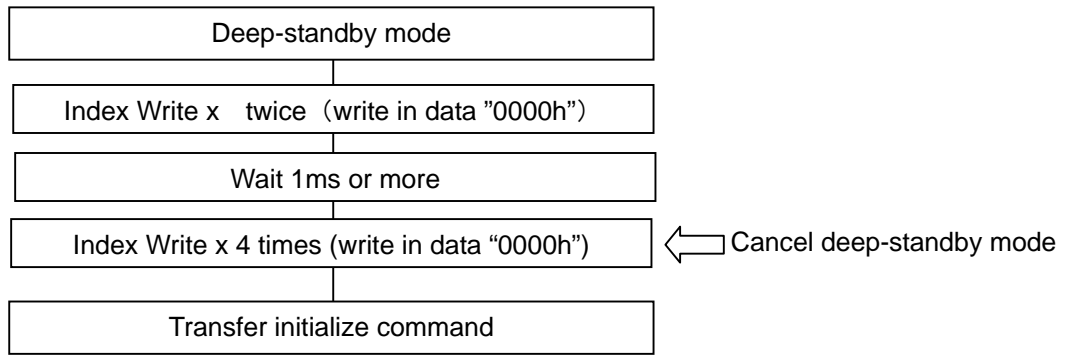


Figure 2 Sequence for exiting deep-standby mode (16 bit interface mode)

(2) 8-/9-bit interface mode

Cancel deep-standby mode by writing bus data "00h" five times and then writing bus data "F0h" once. Make sure to write in "00h" four times consecutively as the transfer synchronization process. Wait 1ms or more between 2nd and 3rd write-in operation.

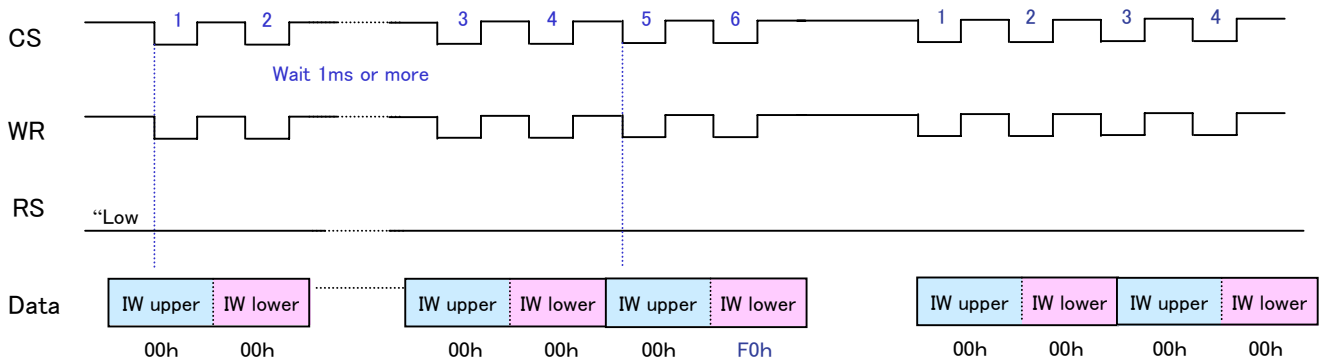


Figure 3 Signal input timings when canceling deep-standby mode (8 bit interface mode) **Transfer synchronization**

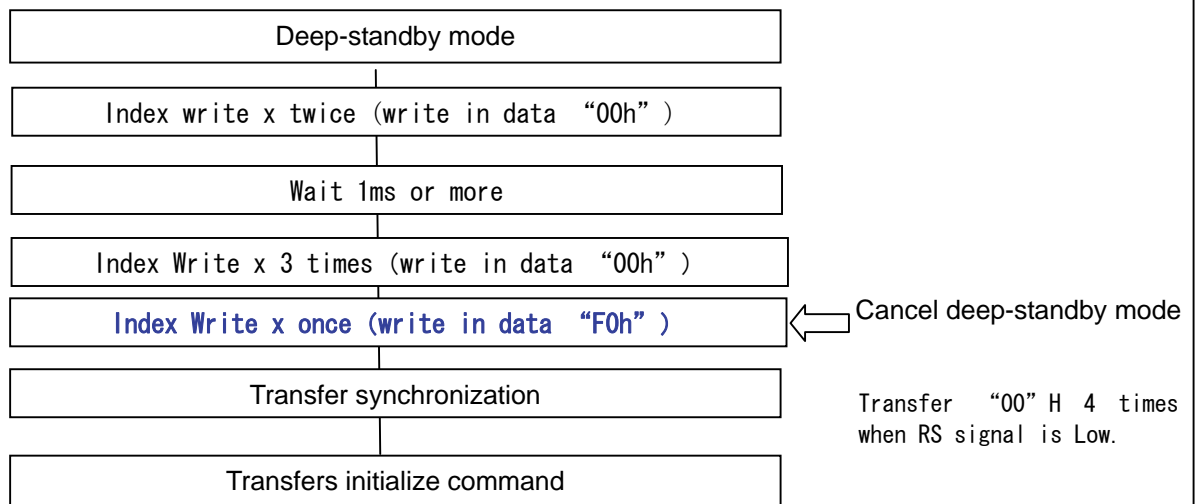


Figure 4 Sequence for exiting deep-standby mode (8 bit interface mode)