To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-R8C-A002B/E	Rev.	2.00
Title	Specification Changes in the R8C/L35A Group, R8C/L35B Group, R8C/L36A Group, R8C/L36B Group, R8C/L38A Group, R8C/L38B Group, R8C/L3AA Group R8C/L3AB Group Hardware Manual		Information Category	Technical Notification		
Applicable Products	R8C/L35A Group, R8C/L35B Group R8C/L36A Group, R8C/L36B Group R8C/L38A Group, R8C/L38B Group R8C/L3AA Group and R8C/L3AB Group	Lot No. __	Reference Document	Described below		

(8) in section 1-1 and section 2-8 have been revised in Revision 2.00.

1. Overview

The below changes have been made to the specifications described in the datasheet and hardware manual of the R8C/L3AA Group, R8C/L3AB Group, R8C/L38A Group, R8C/L38B Group, R8C/L36A Group, R8C/L36B Group, R8C/L35A Group and R8C/L35B Group.

1-1. Changes

(1) Removed the high-speed on-chip oscillator

(2) Changed the flash memory suspend function specifications

(3) Changed the flash memory suspend electrical characteristics

(4) Changed the timer RG specifications

(5) Changed the LCD port specifications

(6) Removed the voltage monitor 0 reset/power-on reset

(7) Removed the voltage monitor 1 /comparator A1 and voltage monitor 2 / comparator A2 functions

(8) Note on reducing power current

1-2. Reference Documents

The information in this document applies to the R8C/L35A Group, R8C/L35B Group, R8C/L36A Group, R8C/L36B Group, R8C/L35A Group, R8C/L38B Group, R8C/L3AA Group, R8C/L3AB Group Hardware Manual Rev.0.30 and Datasheet Rev.0.30.

2. Description

2-1. Removed the High-Speed On-Chip Oscillator

The high-speed on-chip oscillator function has been removed.

Do NOT select the high-speed on-chip oscillator as the clock source for the CPU clock or peripheral functions.

Descriptions regarding the high-speed on-chip oscillator in the reference documents shown in 1-2, other than descriptions shown in this technical update, are invalid.

2-1-1. Register Settings Related to the Clock Generation Circuit

2-1-1-1. High-Speed On-Chip Oscillator Control Register 0 (FRA0)

(1) Do NOT set FRA00 bit to 1 (high-speed on-chip oscillator on) [refer to Figure 2-1]

(2) Do NOT set FRA01 bit to 1 (high-speed on-chip oscillator selected as fOCO clock source) [refer to Figure 2-1].
The fOCO is a clock source of timer RA.

(3) Do NOT set FRA03 bit to 1 (fOCO-F divided by 128 selected as a clock source of fOCO128) [refer to Figure 2-1].
fOCO128 is used as an input-capture signal of timers RC and RD.

2-1-1-2. System Clock Control Register 3 (CM3)

(1) Do NOT set bits CM37 to CM36 bits to 10b (high-speed on-chip oscillator selected as CPU clock when the MCU exits wait mode or stop mode) [refer to Figure 2-2].

2-1-1-3. High-Speed On-Chip Oscillator Control Register i (FRAi) (i = 1 to 7)

(1) Do NOT set the register related to the high-speed on-chip oscillator division select (FRA2) or registers related to frequency adjustment (FRA1 and FRA3 to FRA7).

2-1-2. Register Settings Related to Timer RA

2-1-2-1. High-Speed On-chip Oscillator Control Register 0 (FRA0)

(1) Do NOT set the FRA01 bit to 1 (high-speed on-chip oscillator selected for the fOCO clock) [refer to Figure 2-1]. The high-speed on-chip oscillator clock cannot be selected as the timer RA count source.

2-1-3 Register Settings Related to Timer RC

2-1-3-1. Timer RC Control Register 1 (TRCCR1)

(1) Do NOT set bits TCK2 to TCK0 to 110b (fOCO40M selected as the timer RC count source) [refer to Figure 2-3].

(2) Do NOT set bits TCK2 to TCK0 to 111b (fOCO-F selected as the timer RC count source) [refer to Figure 2-3].

2-1-3-2. High-speed On-Chip Oscillator Control Register 0 (FRA0)

(1) Do NOT set the FRA03 bit to 1 (fOCO-F divided by 128 selected as the fOCO 128 clock) [refer to Figure 2-1]. For the timer RC input-capture function, fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRCGRA register.

2-1-4. Register Settings Related to Timer RD

2-1-4-1. Timer RD Control Register 0, 1 (TRDCR0, TRDCR1)

(1) Do NOT set bits TCK2 to TCK0 to 110b (fOCO40M selected as the timer RD count source) [refer to Figure 2-4].

(2) Do NOT set bits TCK2 to TCK0 to 111b (fOCO-F selected as the timer RD count source) [refer to Figure 2-4].

2-1-4-2. High-speed On-Chip Oscillator Control Register 0 (FRA0)

(1) Do NOT set the FRA03 bit to 1 (fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRDGRA0 register [refer to Figure 2-1]. For the timer RD input-capture function, fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRDGRA register.

2-1-5. Timer RG Control Register Settings

2-1-5-1. Timer RG Control Register (TRGCR)

(1) Do NOT set bits TCK2 to TCK0, the count source select bits in the timer RG control register (TRGCR), to 110b (fOCO40M selected as a count source of timer RG) [refer to Figure 2-5].

2-1-6. Register Settings for the A/D Converter

2-1-6-1. A/D Mode Register (ADMOD)

(1) Do NOT set the CKS2 bit to 1 (fOCO-F selected as the A/D converter operating clock source) [refer to Figure 2-6].

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: ~~High-speed on-chip oscillator on~~ ← Do NOT set.	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: ~~High-speed on-chip oscillator selected~~	R/W
b2	—	Reserved bit	Set to 0. ← Do NOT set.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: ~~fOCO-F divided by 128 selected~~	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0. ← Do NOT set.		—
b5	—			
b6	—			
b7	—			

Notes:

1. Change the FRA01 bit under the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 2.7 V to 5.5 V 000b to 111b
     Divide ratio of 8 or more when VCC = 1.8 V to 5.5 V 110b to 111b (divide-by-8 or more)
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA01 bit to 0 before setting the FRA00 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

Figure 2-1.High-Speed On-Chip Oscillator Control Register 0 (FRA0) Setting

System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division	R/W
b6	CM36	System clock select bit when exiting wait or stop mode	b7 b6 0 0: MCU exits with the CPU clock used immediately before entering wait or stop mode 0 1: Do not set. 1 0: ~~High-speed on-chip oscillator clock selected~~ (3) 1 1: XIN clock selected (4) → Do NOT set.	R/W
b7	CM37			R/W

Notes:

1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. ~~When bits CM37 to CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode:~~
   ~~• OCD2 bit in OCD register = 1 (on-chip oscillator selected)~~
   ~~• FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)~~
   ~~• FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)~~
4. When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OM05 bit in OM0 register = 1 (XIN clock oscillates)
   • OM13 bit in OM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.
   However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

Figure 2-2. System Clock Control Register 3 (CM3) Setting

Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: ~~TRCCLK input rising edge~~ 1 1 0: ~~fOCO40M~~ 1 1 1: fOCO-F (2)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: TRC counter cleared by input capture or by compare match with the TRCGRA register	R/W

Do NOT set.

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. ~~To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency~~

Figure 2-3. Timer RC Control Register 1 (TRCCR1) Setting

Timer RD Control Register i (TRDCRi) (i = 0 or 1)

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: ~~fOCO40M~~ 1 1 1: ~~fOCO-F (5)~~	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	b7 b6 b5 0 0 0: Clear disabled (free-running operation) 0 0 1: Clear by input capture to the TRDGRAi register 0 1 0: Clear by input capture to the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (4) 1 0 0: Do not set. 1 0 1: Clear by input capture to the TRDGRCi register 1 1 0: Clear by input capture to the TRDGRDi register 1 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Do NOT set.

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2) in timer mode.
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
4. Enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).
5. ~~To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency~~.

Figure 2-4. Timer RD Control Register 0,1 (TRDCR0, TRDCR1) Setting

Timer RG Control Register (TRGCR)

Address 0172h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit (1)	b2 b1 b0 0 0 0: f1 ~~0 0 1: f2~~ Do NOT set. See 2-4. 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRGCLKA input ~~1 1 0: fOCO40M~~ Do NOT set. See 2-1-5-1. 1 1 1: TRGCLKB input	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock active edge select bit (1)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both the rising/falling edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 0: Clear disabled 0 1: TRG register cleared by input capture or compare match with TRGGRA register 1 0: TRG register cleared by input capture or compare match with TRGGRB register 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Note:
1. In phase counting mode, the settings of bits TCK0 to TCK2 and bits CKEG0 and CKEG1 are disabled and the operation of phase counting mode has priority.

Figure 2-5. Timer RG Control Register (TRGCR) Setting

A/D Mode Register (ADMOD)

Address 00D4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 0 0: fAD divided by 8 0 1: fAD divided by 4 1 0: fAD divided by 2 1 1: fAD divided by 1 (no division)	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit (1)	0: f1 selected ~~1: fOCO-F selected~~ ← Do NOT set.	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3 0 0 0: One-shot mode 0 0 1: Do not set. 0 1 0: Repeat mode 0 0 1 1: Repeat mode 1 1 0 0: Single sweep mode 1 0 1: Do not set. 1 1 0: Repeat sweep mode 1 1 1: Do not set.	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion starts by software trigger (ADST bit in ADCON0 register) 0 1: A/D conversion starts by conversion trigger from timer RD 1 0: A/D conversion starts by conversion trigger from timer RC 1 1: A/D conversion starts by external trigger (ADTRG)	R/W
b7	ADCAP1			R/W

Note:
1. When the CKS2 bit is changed, wait for three ϕAD cycles or more before starting A/D conversion.

If the content of the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

Figure 2-6. A/D Mode Register (ADMOD) Setting

2-2. Changes in the Flash Memory Suspend Function

Flash programming operation is disabled when the auto-erasure is suspended while using the flash memory suspend function.

Executable Operation during Suspend

		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	×	×	×	×	~~○~~	○	—	—	—	×	~~○~~	○(5)
	Program ROM	—	—	—	×	~~○~~	○	×	×	×	×	~~○~~	○

Notes:

1. ○ indicates operation is enabled by using the suspend function, × indicates operation is disabled, and — indicates no combination is available.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The operation of block blank check is disabled during suspend.
4. The MCU enters read array mode immediately after entering erase-suspend.
5. The program ROM area can be read with the BGO function while programming or block erasing data flash.

Program is also not available with Data Flash driver in condition indicated in .

Figure 2-7. Flash Memory Suspend Function

2-3. Changes in the Flash Memory Suspend Function Electrical Characteristics

Wait for at least 33 ms after the erase start/restart request before the making the next erase/suspend request. This is described as the “Interval from erase start/restart until suspend” in the hardware manual [refer to Figure 2-7].

Flash Memory (Program ROM) Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.)

–	Interval from erase start/restart until following suspend request		~~0~~ →33	–	–	~~µs~~ →ms
–	Suspend interval necessary for auto-erasure to complete		33	–	–	ms

Flash Memory (Data flash Block A to Block D) Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

–	Interval from erase start/restart until following suspend request		~~0~~ →33	–	–	~~µs~~ →ms
–	Suspend interval necessary for auto-erasure to complete		33	–	–	ms

Figure 2-8. Flash Memory Suspend Electrical Characteristics

2-4. Change in the Timer RG Function

Do NOT set the count source select bits (TCK2 to TCK0) in the timer RG control register (TRGCR) to 001b (f2 selected as the count source of timer RG) [refer to Figure 2-5].

2-5. Changes in the LCD Port Function

2-5-1. LCD Port Select Register 0 (LSE0)

This information applies to the R8C/L35A Group, R8C/L36A Group, R8C/L35B Group, and R8C/L36B Group.

Do NOT set bits LSE06 and LSE07 to 1 (SEG6 and SEG7 port functions selected). P0_6/SEG6 and P0_7/SEG7 cannot be used as segment pins SEG6 and SEG7. P0_6/SEG6 and P0_7/SEG7 can be used as I/O ports P0_6 and P0_7.

2-5-2. LCD Port Select Register 2 (LSE2)

This information applies to the R8C/L38A Group and R8C/L38B Group.

Do NOT set the LSE16 bit to 1 (SEG16 port function selected). P2_0/SEG16/KI0 cannot be used as segment pin SEG16. P2_0/SEG16/KI0 can be used as I/O port P0_2 and KI0.

2-6. Voltage Monitor 0 Reset and Power-On Reset

The voltage monitor 0 reset and power-on reset cannot be used. Use a hardware reset to reset the MCU. In the documents listed in section 1-2, descriptions of the voltage monitor 0 reset and power-on reset are invalid.

2-7. Removed the Voltage Monitor 1 / Comparator A1 Interrupt and Voltage Monitor 2 / Comparator A2 Interrupt Functions

Voltage monitor 1 / comparator A1 and voltage monitor 2 / comparator A2 cannot be used. In the documents listed in section 1-2, description of the voltage monitor 0 reset or power-on reset are invalid.

2-8. Note on Reducing Power Current

Write 00h to the POMCR0 register (address 0020h) by a program. Current consumption may increase until 00h is written to the POMCR0 register.

Sample code: MOV.B #00H, 0020H

3. Other Note

Note regarding pins P12_1 and P12_0.

P12_1 and P12_0 are shared with XIN and XOUT. When XIN is used as a clock, these ports cannot be used as I/O ports.

4. Slated Changes

Contact the Renesas Technology sales department for schedule and products with high-speed on-chip oscillator.

- End of description -