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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU & MCU | | Document No. | TN-RX*-A110A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Specification Changes to Improve the Products in the RX111 Group | | Information Category | Technical Notification | | |
| Applicable Product | RX111 Group<br>Products with #3A or #UA at the end of the orderable part number | Lot No.<br>All | Reference Document | RX111 Group User's Manual: Hardware Rev.1.10 (R01UH0365EJ0110)<br>Corrections to Descriptions for the Flash Memory in the RX111 Group User's Manual (TN-RX*-A109A/E) | | |

This document describes changes to the specifications in RX111 Group User's Manual: Hardware Rev.1.10 for the improvement of the products in the RX111 Group. The specifications for the improved products are changed as follows:

- Changed orderable part numbers
- Added an option for sub-clock oscillator drive capacity
- Relax the restriction on AVCC0
- Added the temperature sensor calibration data registers
- Added the unique ID

## 1. Changed Orderable Part Numbers

The end of orderable part numbers are changed from #30 and #U0 to #3A and #UA, respectively.

For example,

R5F51115AGFM#30 → R5F5115AGFM#3A

R5F51114ADLF#U0 → R5F51114ADLF#UA

## 2. Added an Option for Sub-Clock Oscillator Drive Capacity

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"Drive capacity for a standard-CL crystal" is added to the Description column of the RTCDV[2:0] bits in 23.2.19 RTC Control Register 3 (RCR3) and descriptions for setting values are also changed as follows:

Before correction

| bit | symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b3 to b1 | RTCDV[2:0] | Sub-Clock Oscillator Drive Capacity Control | b3 b1<br>0 0 0: Medium drive capacity (4.4 pF type)<br>0 0 1: High drive capacity (6.0 pF type)<br>1 0 1: Low drive capacity (3.7 pF type)<br>Settings other than above are prohibited. | R/W |

After correction

| bit | symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b3 to b1 | RTCDV[2:0] | Sub-Clock Oscillator Drive Capacity Control | b3 b1<br>0 0 0: Medium drive capacity for a low-CL crystal<br>0 0 1: High drive capacity for a low-CL crystal<br>0 1 0: Low drive capacity for a low-CL crystal<br>1 0 0: Drive capacity for a standard-CL crystal<br>Settings other than above are prohibited. | R/W |

## 3. Relax the Restriction on AVCC0

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Description for port 4 and port J in Table 18.7 Handling of Unused Pins is changed as follows:

Before correction

| Pin Name | Description |
|---|---|
| Port 0 to 5, A to C, E, H, J (for pins that exist on products with fewer than 64 pins) | • Set these pins to input (PORTn.PDR bit = 0) and connect each of them to VCC via a pull-up resistor or to VSS via a pull-down resistor. *1<br>• Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open. *1, *2 |

After correction

| Pin Name | Description |
|---|---|
| Ports 0 to 3, 5, A to C, E, H (for pins that exist on products with fewer than 64 pins) | • Set these pins to input (PORTn.PDR bit = 0) and connect each of them to VCC via a pull-up resistor or to VSS via a pull-down resistor. *1<br>• Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open. *1, *2 |
| Ports 4 and J (for pins that exist on products with fewer than 64 pins) | • Set these pins to input (PORTn.PDR bit = 0) and connect each of them to AVCC0 via a pull-up resistor or to AVSS0 via a pull-down resistor. *1<br>• Set these pins to output (PORTn.PDR bit = 1), set the output data to 0 (PORTn.PODR bit = 0), and leave them open. *1, *2 |

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Descriptions for “Relationship between power supply pin pairs (AVCC0–AVSS0, VREFH0–VREFL0, VCC–VSS)” of the second bullet in 30.7.10 are changed as follows:

Before correction

The following conditions should be satisfied: AVCC0 = VCC, and AVSS0 = VSS. A 0.1-µF capacitor should be connected between each pair of power supply pins to create a closed loop with the shortest route possible as shown in Figure 30.16, and connection should be made so that the following conditions are satisfied at the supply side.
VREFL0 = AVSS0 = VSS
When the A/D converter is not used, the following conditions should be satisfied.
VREFH0 = AVCC0 = VCC and VREFL0 = AVSS0 = VSS

After correction

The following condition should be satisfied: AVSS0 = VSS. A 0.1-µF capacitor should be connected between each pair of power supply pins to create a closed loop with the shortest route as shown in Figure 30.16, and connection should be made so that the following conditions are satisfied at the supply side:
VREFL0 = AVSS0 = VSS
When the 12-bit A/D converter is not used, the following conditions should be satisfied:
VREFH0 = AVCC0 = VCC and VREFL0 = AVSS0 = VSS

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Specifications for AVCC0 in Table 36.2 Recommended Operating Conditions are changed as follows:

Before correction

**Table 36.2 Recommended Operating Conditions**

| Item | Symbol | Value | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltages | VCC | When USB not used | 1.8 | — | 3.6 | V |
| | | When USB used | 3.0 | — | 3.6 | V |
| | VSS | | — | 0 | — | V |
| USB power supply voltages | VCC_USB | | — | VCC | — | V |
| | VSS_USB | | — | 0 | — | V |
| Analog power supply voltages | AVCC0 *1 | | — | VCC | — | V |
| | AVSS0 | | — | 0 | — | V |

Note 1. For details, 30.7.10 Voltage Range of Analog Power Supply Pins.

After correction

**Table 36.2 Operating Conditions**

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltages | VCC *1 | When USB not used | 1.8 | — | 3.6 | V |
| | | When USB used | 3.0 | — | 3.6 | V |
| | VSS | | — | 0 | — | V |
| USB power supply voltages | VCC_USB | | — | VCC | — | V |
| | VSS_USB | | — | 0 | — | V |
| Analog power supply voltages | AVCC0 *1, *2 | | 1.8 | — | 3.6 | V |
| | AVSS0 | | — | 0 | — | V |

Note 1. Supply AVCC0 simultaneously with or after supplying VCC.
Note 2. Refer to section 30.7.10, Voltage Range of Analog Power Supply Pins to determine the AVCC0 voltage.

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Condition for AVCC0 in Table 36.3 DC Characteristics (1) and specifications for port 4 and port J are changed as follows:

Before correction

**Table 36.3 DC Characteristics (1)**

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | *omitted* | | | | | | |
| Input level voltage (except for Schmitt trigger input pins) | MD | $V_{IH}$ | VCC × 0.9 | — | VCC + 0.3 | V | |
| | XTAL (external clock input) | | VCC × 0.8 | — | VCC + 0.3 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | VCC × 0.7 | — | VCC + 0.3 | | |
| | RIIC input pin (SMBus) | | 2.1 | — | VCC + 0.3 | | |
| | MD | $V_{IL}$ | –0.3 | — | VCC × 0.1 | | |
| | XTAL (external clock input) | | –0.3 | — | VCC × 0.2 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | –0.3 | — | VCC × 0.3 | | |
| | RIIC input pin (SMBus) | | –0.3 | — | 0.8 | | |

After correction

**Table 36.3 DC Characteristics (1)**

Conditions: VCC = VCC_USB = 2.7 to 3.6 V, AVCC0 = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
$T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | *omitted* | | | | | | |
| Input level voltage (except for Schmitt trigger input pins) | MD | $V_{IH}$ | VCC × 0.9 | — | VCC + 0.3 | V | |
| | XTAL (external clock input) | | VCC × 0.8 | — | VCC + 0.3 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | AVCC0 × 0.7 | — | AVCC0 + 0.3 | | |
| | RIIC input pin (SMBus) | | 2.1 | — | VCC + 0.3 | | |
| | MD | $V_{IL}$ | –0.3 | — | VCC × 0.1 | | |
| | XTAL (external clock input) | | –0.3 | — | VCC × 0.2 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | –0.3 | — | AVCC0 × 0.3 | | |
| | RIIC input pin (SMBus) | | –0.3 | — | 0.8 | | |

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Condition for AVCC0 in Table 36.4 DC Characteristics (2) and specifications for port 4 and port J are changed as follows:

Before correction

**Table 36.4 DC Characteristics (2)**

Conditions: VCC = AVCC0 = VCC_USB = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = VSS_USB = 0 V,
$T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | *omitted* | | | | | | |
| Input level voltage (except for Schmitt trigger input pins) | MD | $V_{IH}$ | VCC × 0.9 | — | VCC + 0.3 | V | |
| | XTAL (external clock input) | | VCC × 0.8 | — | VCC + 0.3 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | VCC × 0.7 | — | VCC + 0.3 | | |
| | MD | $V_{IL}$ | –0.3 | — | VCC × 0.1 | | |
| | XTAL (external clock input) | | –0.3 | — | VCC × 0.2 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | –0.3 | — | VCC × 0.3 | | |

After correction

**Table 36.4 DC Characteristics (2)**

Conditions: VCC = VCC_USB = 1.8 to 2.7 V, AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
$T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | *omitted* | | | | | | |
| Input voltage (except for Schmitt trigger input pins) | MD | $V_{IH}$ | VCC × 0.9 | — | VCC + 0.3 | V | |
| | XTAL (external clock input) | | VCC × 0.8 | — | VCC + 0.3 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | AVCC0 × 0.7 | — | AVCC0 + 0.3 | | |
| | MD | $V_{IL}$ | –0.3 | — | VCC × 0.1 | | |
| | XTAL (external clock input) | | –0.3 | — | VCC × 0.2 | | |
| | Ports 40 to 44, 46, ports J6, J7 | | –0.3 | — | AVCC0 × 0.3 | | |

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Condition for AVCC0 in Table 36.17 Output Values of Voltage (1) and specifications for port 4 and port J are changed as follows:

Before correction

**Table 36.17 Output Values of Voltage (1)**

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output low | *omitted* | | | | | |
| Output high | All output ports (except for port 4 and port J) | $V_{OH}$ | VCC – 0.5 | — | V | $I_{OH}$ = –2.0 mA |
| | Ports 40 to 44, 46, ports J6, J7 | | VCC – 0.5 | — | | $I_{OH}$ = –0.1 mA |

After correction

**Table 36.17 Output Voltage (1)**

Conditions: VCC = VCC_USB = 2.7 to 3.6 V, AVCC0 = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
$T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Low-level output voltage | *omitted* | | | | | |
| High-level output voltage | All output ports (except for port 4 and port J) | $V_{OH}$ | VCC – 0.5 | — | V | $I_{OH}$ = –2.0 mA |
| | Ports 40 to 44, 46, ports J6, J7 | | AVCC0 – 0.5 | — | | $I_{OH}$ = –0.1 mA |

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Condition for AVCC0 in Table 36.18 Output Values of Voltage (2) and specifications for port 4 and port J are changed as follows:

Before correction

**Table 36.18 Output Values of Voltage (2)**

Conditions: VCC = AVCC0 = VCC_USB = 1.8 to 2.7 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output low | *omitted* | | | | | |
| Output high | All output ports (except for port 4 and port J) | $V_{OH}$ | VCC – 0.5 | — | V | $I_{OH}$ = –1.0 mA |
| | Ports 40 to 44, 46, ports J6, J7 | | VCC – 0.5 | — | | $I_{OH}$ = –0.1 mA |

After correction

**Table 36.18 Output Voltage (2)**

Conditions: VCC = VCC_USB = 1.8 to 2.7 V, AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
$T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Low-level output voltage | *omitted* | | | | | |
| High-level output voltage | All output ports (except for port 4 and port J) | $V_{OH}$ | VCC – 0.5 | — | V | $I_{OH}$ = –1.0 mA |
| | Ports 40 to 44, 46, ports J6, J7 | | AVCC0 – 0.5 | — | | $I_{OH}$ = –0.1 mA |

## 4. Added the Temperature Sensor Calibration Data Registers

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Table 5.1 List of I/O Registers (Address Order) (16/16) in 5. I/O Registers is changed as follows:

Before correction

**Table 5.1 List of I/O Registers (Address Order) (16/16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | Reference Section |
|---|---|---|---|---|---|---|---|
| 000A 0096h | USB0 | PIPE2 Transaction Counter Register | PIPE2TRN | 16 | 16 | 9 PCLKB or more | section 25. |
| | | | *omitted* | | | | |
| 007F C090h | FLASH | E2 DataFlash Control Register | DFLCTL | 8 | 8 | 2 or 3 FCLK | section 35. |
| 007F C0B0h | FLASH | Flash Start-Up Setting Monitor Register | FSCMR | 16 | 16 | 2 or 3 FCLK | section 35. |
| | | | *omitted* | | | | |

After correction

**Table 5.1 List of I/O Registers (Address Order) (16/16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | Reference Section |
|---|---|---|---|---|---|---|---|
| 000A 0096h | USB0 | PIPE2 Transaction Counter Register | PIPE2TRN | 16 | 16 | 9 PCLKB or more | section 25. |
| | | | *omitted* | | | | |
| 007F C090h | FLASH | E2 DataFlash Control Register | DFLCTL | 8 | 8 | 2 or 3 FCLK | section 35. |
| 007F C0ACh | TEMPS | Temperature Sensor Calibration Data Register | TSCDRL | 8 | 8 | 1 or 2 PCLKB | section 32. |
| 007F C0ADh | TEMPS | Temperature Sensor Calibration Data Register | TSCDRH | 8 | 8 | 1 or 2 PCLKB | section 32. |
| 007F C0B0h | FLASH | Flash Start-Up Setting Monitor Register | FSCMR | 16 | 16 | 2 or 3 FCLK | section 35. |
| | | | *omitted* | | | | |

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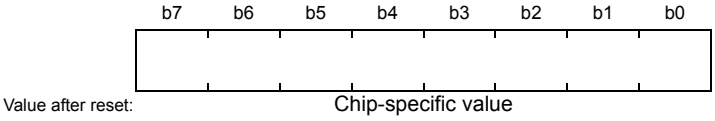
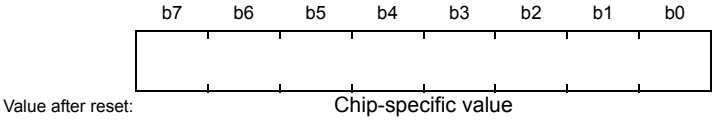
Section 32.2 Register Descriptions and registers below are added to 32. Temperature Sensor (TEMPSa).

### 32.2.1 Temperature Sensor Calibration Data Register (TSCDRH, TSCDRL)

Address(es): TSCDRL 007F C0ACh




Address(es): TSCDRH 007F C0ADh




Registers TSCDRH and TSCDRL stores the temperature sensor calibration data that was measured for each individual chip before shipping.

The temperature sensor calibration data is a digital value (converted by the 12-bit A/D converter) of the voltage that the temperature sensor outputs under the following conditions: Ta = Tj = 88°C, and AVCC0 = VREFH0 = 3.3 V. The TSCDRH register stores the upper 4 bits, and the TSCDRL register stores the lower 8 bits.

## 5. Added the Unique ID

The unique ID is added to each product for identifying the individual MCU. Accordingly, the unique ID register is added, and “consecutive read command” is changed to “unique ID read command”.

### 5.1 Added the Unique ID Register

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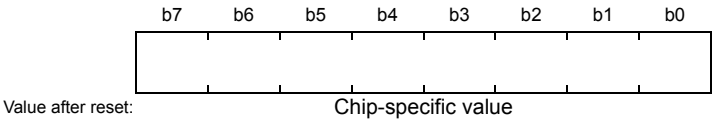
The unique ID register is added to 35. Flash Memory as follows:

#### 35.4.26 Unique ID Register n (UIDRn) (n = 0 to 31)

Address(es): 0850h to 086Fh (extra area)




The UIDRn register stores 32-byte ID code (unique ID) for identifying the individual MCU.
The unique ID is stored in the extra area of the flash memory and cannot be rewritten by the user.
Use the unique ID read command to read the register value.

### 5.2 Changed from “Consecutive Read Command” to “Unique ID Read Command”

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The Software commands column in Table 35.1 Flash Memory Specifications is changed as follows:

Before correction

**Table 35.1 Flash Memory Specifications**

| Item | Description |
|---|---|
| Memory space | *omitted* |
| Software commands | • The following commands can be executed in boot mode or during self-programming: blank check, block erase, program, read, set access window<br>*omitted* |
| | *omitted* |

After correction

**Table 35.1 Flash Memory Specifications**

| Item | Description |
|---|---|
| Memory space | *omitted* |
| Software commands | • The following commands can be executed in boot mode or during self-programming: blank check, block erase, program, unique ID read, set access window<br>*omitted* |
| | *omitted* |

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Descriptions in 35.4.1 E2 DataFlash Control Register (DFLCTL) are changed as follows:

Before correction

| bit | symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b0 | DFLEN | E2 DataFlash Access Enable | 0: Access to E2 DataFlash and access to code flash in P/E mode*1 disabled<br>1: Access to E2 DataFlash and access to code flash in P/E mode*1 enabled | R/W |
| b7 to b1 | — | Reserved | These bits are read as 0. The write value should be 0. | R/W |

Note 1. Consecutive reading and start-up area information programming/access window information programming in P/E mode

The DFLCTL register is used to enable or disable accessing (reading, programming, and erasing) of the E2 DataFlash and accessing (consecutive reading and start-up area information programming/access window information programming) of the code flash.

After correction

| bit | symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b0 | DFLEN | E2 DataFlash Access Enable | 0: Access to E2 DataFlash and access to the extra area in P/E mode*1 disabled<br>1: Access to E2 DataFlash and access to the extra area in P/E mode*1 enabled | R/W |
| b7 to b1 | — | Reserved | These bits are read as 0. The write value should be 0. | R/W |

Note 1. Unique ID read, start-up area information program, and access window information program

The DFLCTL register is used to enable or disable access (read, program, and erase) to the E2 DataFlash and access (unique ID read, start-up area information program, and access window information program) to the extra area in P/E mode.

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Descriptions in 35.4.9 Flash Control Register (FCR) are changed as follows:

Before correction

| bit | symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b3 to b0 | CMD[3:0] | Software Command Setting | b3 b0<br>0 0 0 1:Program<br>0 1 0 0:Block erase<br>0 1 0 1:Consecutive read<br>0 0 1 1:Blank check<br>Settings other than above are prohibited.*1 | R/W |
| b4 | DRC | Data Read Completion | 0: Data is not read or next data is requested.<br>1: Data reading is completed. | R/W |
| | | | *omitted* | |

Note 1. This does not include writing 00h to the FCR register when the FSTATR1.FRDY bit is 1.

— *omitted* —

[Products with 384-Kbyte or 512-Kbyte ROM]

• Consecutive reading and blank checking cannot be executed across 256-Kbyte boundaries.

After correction

| bit | symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b3 to b0 | CMD[3:0] | Software Command Setting | b3 b0<br>0 0 0 1:Program<br>0 0 1 1:Blank check<br>0 1 0 0:Block erase<br>0 1 0 1:Unique ID read<br>Settings other than above are prohibited.*1 | R/W |
| b4 | DRC | Data Read Completion | 0: Start data read.<br>1: Complete data read. | R/W |
| | | | *omitted* | |

Note 1. This does not include set the FCR register to 00h when the FSTATR1.FRDY flag is 1.

— *omitted* —

[Products with 384-Kbyte or 512-Kbyte ROM]

• Blank check cannot be executed across 256-Kbyte boundaries.

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Descriptions for bits CMD[3:0] and DRC in 35.4.9 Flash Control Register (FCR) are changed as follows:

Before correction

**CMD[3:0] Bits (Software Command Setting)**

These bits are used to set a software command (program, block erase, consecutive read, or blank check).
The function of each command is described below.
— *omitted* —
[Consecutive read]

- Read the area from the address set in the FSARH and FSARL registers to the address set in the FEARH and FEARL registers during ROM read P/E mode or E2 DataFlash P/E mode. The read data is stored in the FRBH and FRBL registers.

**DRC Bit (Data Read Completion)**

After executing a consecutive read command and reading the FRBH and FRBL registers, write 1 to the DRC bit to complete the processing for reading the data. To issue a request for reading the next data, write 0 to the DRC bit.

After correction

**CMD[3:0] Bits (Software Command Setting)**

These bits are used to set a software command (program, block erase, unique ID read, or blank check).
The function of each command is described below.
— *omitted* —
[Unique ID read]

- When executing the unique ID read after setting registers FSARH, FSARL, FEARH, and FEARL to 00h, 0850h, 00h, and 086Fh, respectively, the unique ID is stored in registers FRBH and FRBL sequentially.

**DRC Bit (Data Read Completion)**

This bit is used with the unique ID read command to control the state of the sequencer.
When issuing the unique ID read command with this bit set to 0, data is read from the address set in registers FSARH and FSARL, and the data is stored in registers FRBH and FRBL.
When issuing the unique ID read command with this bit set to 1 after reading data from registers FRBH and FRBL, the sequencer ends the read cycle and enters the wait state.
When issuing the unique ID read command again with this bit set to 0, the internal address of the sequencer is incremented by 4, and the next data is read.

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Descriptions in 35.4.15 Flash Read Buffer Register H (FRBH) are changed as follows:

Before correction

This register is used to store the higher-order 16 bits of the data read from the ROM when consecutive read is executed. When the E2 DataFlash is read, the read data is stored in bit 7 to bit 0 in the FRBL register.

After correction

This register is used to store the upper 2 bytes of the 4-byte data (part of the unique ID) that is read from the extra area when unique ID read is executed.

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Descriptions in 35.4.16 Flash Read Buffer Register L (FRBL) are changed as follows:

Before correction

This register is used to store the lower-order 16 bits of the data read from the ROM or the data read from the E2 DataFlash when consecutive read is executed.
When the E2 DataFlash is read, 00h is stored in bit 15 to bit 8.

After correction

This register is used to store the lower 2 bytes of the 4-byte data (part of the unique ID) that is read from the extra area when unique ID read is executed.

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Descriptions for the DRRDY flag is added to 35.4.20 Flash Status Register 1 (FSTATR1) as follows:

**DRRDY Flag (Data Read Ready Flag)**

This flag is used to check if the valid read data is stored in registers FRBH and FRBL.
When the sequencer stores data read from the flash memory to registers FRBH and FRBL, the DRRDY flag becomes 1. When issuing the unique ID command with the FCR.DRC bit set to 1, the sequencer ends the read cycle, and the DRRDY flag becomes 0.
Note that, even if issuing the unique ID command with the FCR.DRC bit set to 0 after reading data from the address set in registers FEARH and FEARL, the DRRDY flag does not become 1, but the FRDY flag becomes 1.

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Table 35.4 Software Commands is changed as follows:

Before correction

**Table 35.4 Software Commands**

| Command | Function |
|---|---|
| | *omitted* |
| Consecutive read | Read the specified area during ROM P/E mode or E2 DataFlash P/E mode. |
| | *omitted* |

After correction

**Table 35.4 Software Commands**

| Command | Function |
|---|---|
| | *omitted* |
| Unique ID read | Read the unique ID from the extra area |
| | *omitted* |

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(5) Consecutive Read in 35.7.3 Software Command Usage is changed as follows:

Before correction

(5) Consecutive Read

Figure 35.17 is a simple flowchart for the procedure for consecutive read.

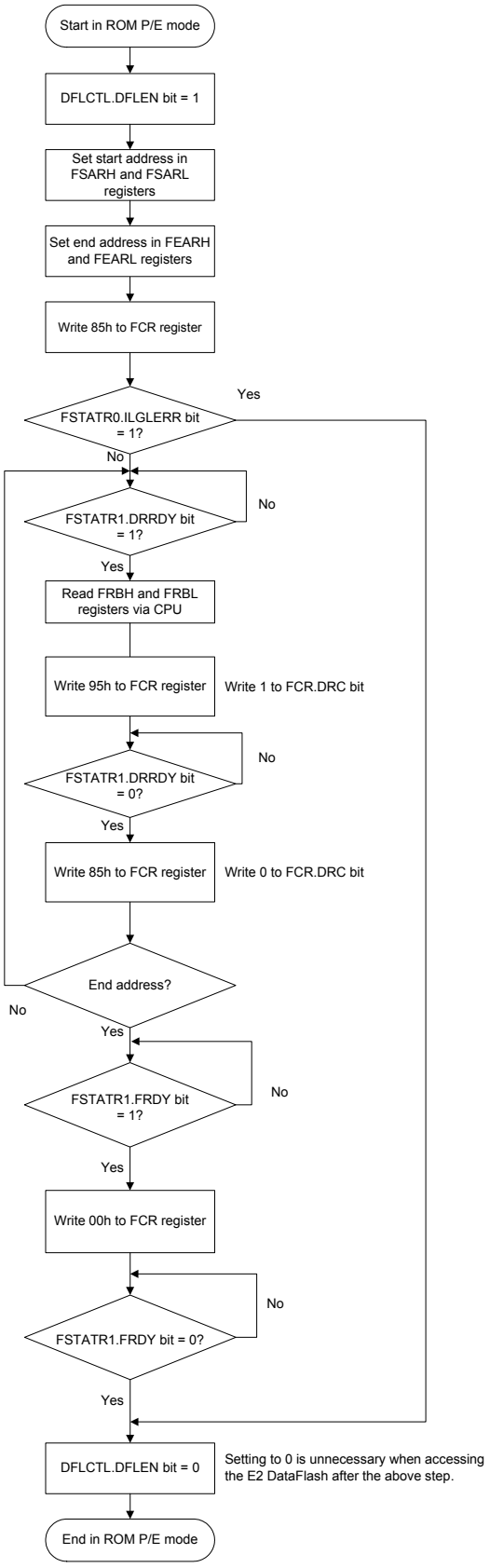


**Figure 35.17 Simple Flowchart of the Procedure for Consecutive Read**

After correction

(5) Unique ID Read

Figure 35.17 is the procedure to issue the unique ID read command.

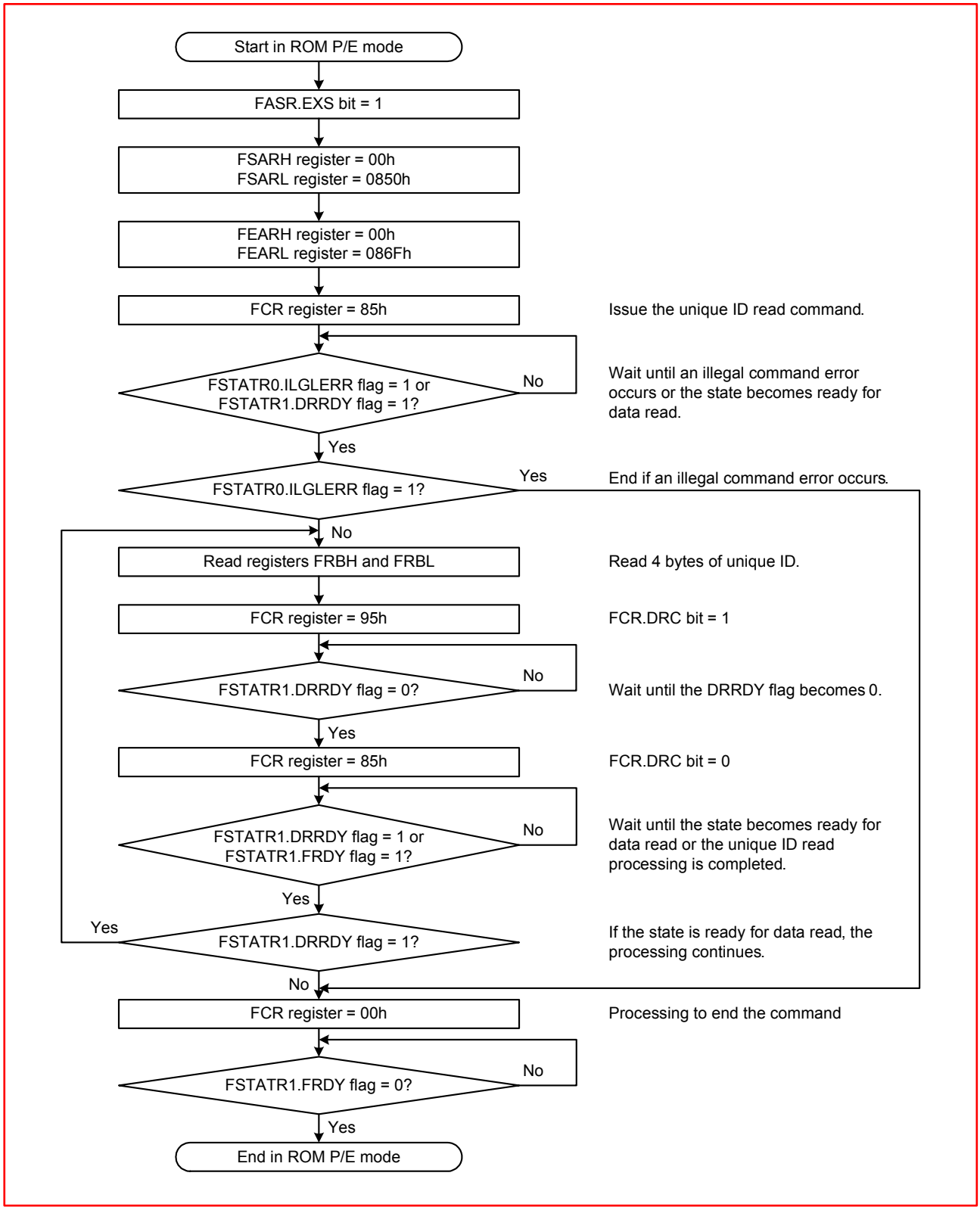


**Figure 35.17 Procedure to Issue the Unique ID Read Command**