To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A411A/E	Rev.	1.00
Title	Specification change of H8S/20103,H8S/20203,H8S/20223 Group internal High-speed On-chip oscillator		Information Category	Technical Notification		
Applicable Product	H8S/20103,H8S/20203,H8S/20223 Group	Lot No. All lots	Reference Document	H8S/20103,H8S/20203,H8S/20223 Group Hardware manual REJ09B0465-0100 (Rev.1.00)		

1. Specification change

High-speed On-chip oscillator (OCO) is removed in H8S/20103, H8S/20203, H8S/20223 Group.

Please do not select high-speed OCO for CPU and peripheral module clock.

High-speed OCO registers should be set as follows.

2. Setting of High-speed OCO registers

2.1 clock generation circuit

(1) Please clear the HOCOE bit of High-Speed OCO Control Register (HOCR) to 0.

5.2.7 High-Speed OCO Control Register (HOCR)

Address: H'FF062A

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	HOCOE	–	–	–	–	–	–	–
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	HOCOE	High-speed OCO enable	0: The high-speed OCO is not used (standby state). 1: ~~The high-speed OCO is used.~~ Setting prohibited.	R/W

(2) High-speed OCO can not be selected for system clock ϕhigh.

Please set the PHISEL bit of System Clock Control Register (SYSCCR) to 1(select ϕosc).

5.2.2 System Clock Control Register (SYSCCR)

Address: H'FF06D0

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	PHIHSEL	PHILSEL	–	SUBNC[1:0]		–
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
5	PHIHSEL	ϕhigh clock source select	0: ϕ~~hoco~~ Setting prohibited. 1: ϕosc [Setting condition] When 1 is written to this bit while CKSWIF in BAKCR is 0. [Clearing conditions] •When 0 is written to this bit. •When the main oscillator stop state is detected while the system clock selects ϕosc and OSCBAKE and BAKCKSEL in BAKCR are 1, respectively.	R/W

(3) When using the backup function, high-speed OCO can not be selected for backup destination clock source.

Please clear the BACKSEL bit of Backup Control Register (BACKR) to 0 (select ϕlow).

5.2.1 Backup Control Register (BACKR)

Address: H'FF06D4

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	OSCBAKE	BAKCKSEL	CKSWIE	CKSWIF	OSCHLT	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
4	BAKCKSEL	Backup destination clock source select	0: ϕlow 1: ~~ϕhoco~~ Setting prohibited.	R/W

(4) Please do not write to below registers on high-speed OCO trimming.

High-Speed OCO Trimming Data Protect Register (HOTRMDPR: address H'FF062B)

High-Speed OCO Trimming Data Register 1 (HOTRMDR1: address H'FF062C)

High-Speed OCO Trimming Data Register 2 (HOTRMDR2: address H'FF062D)

2.2 Timer RA

HOCO clock ϕ40 can not be selected for Timer RA counting source.

Please set TCK[2:0] of Timer RA mode Register(TRAMR) except to "010" .

13.2.3 Timer RA Mode Register (TRAMR)

Address: H'FF06F2

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	TCKCUT	TCK[2:0]			—	TMOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
6 to 4	TCK[2:0]*2	Timer RA count source select	000: φ 001: φ/8 010: ~~φ/40~~ Setting prohibited. 011: φ/2 100: φsub 101: φ/32 110: φ/64 111: φ/128	R/W

2.3 Timer RC (only applicable to H8S/20103 Group)

(1) HOCO clock φ40 can not be selected for Timer RC counting source.

Please set CKS[2:0] of Timer RC Control Register 1 (TRCCR1) except to “110” .

15.2.2 Timer RC Control Register 1 (TRCCR1)

Address: H'FFFF8B

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	CCLR	CKS[2:0]			TOD	TOC	TOB	TOA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
6 to 4	CKS[2:0]*3	Clock select 2 to 0	Select the source of the clock input to TRCCNT. 000: TRCCNT counts the internal clock φ. 001: TRCCNT counts the internal clock φ/2. 010: TRCCNT counts the internal clock φ/4. 011: TRCCNT counts the internal clock φ/8. 100: TRCCNT counts the internal clock φ/32. 101: TRCCNT counts the rising edge of the external event (FTCI). 110: ~~TRCCNT counts the internal clock φ40.*1~~ Setting prohibited. 111: Reserved (setting prohibited)	R/W

2.4 Timer RD

(1) High-speed OCO clock φ40 can not be selected for Timer RD counting source.

Please set TPSC[2:0] of Timer RD Control Register (TRDCR) except to “110” (internal clock count by φ40).

This limitation is applicable to both of 2 units of Timer RD in H8S/20203 Group and H8S/20223Group.

16.2.11 Timer RD Control Register (TRDCR)

Address: H'FFFFCA, H'FFFFD1

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
2 to 0	TPSC[2:0] *3*4	Time prescaler 2 to 0	000: Internal clock: count by φ 001: Internal clock: count by φ/2 010: Internal clock: count by φ/4 011: Internal clock: count by φ/8 100: Internal clock: count by φ/32 101: External clock: count by FTIOA0 (TCLK) pin input 110: ~~Internal clock: count by φ40~~ Setting prohibited. 111: Reserved (setting prohibited)	R/W

2.5 Timer RG

(1) High-speed OCO clock φ40 can not be selected for Timer RG counting source. Please set TPSC[2:0] of Timer RG Control Register (TRGCR) except to “110” .

18.2.3 Timer RG Control Register (TRGCR)

Address: H'FF0648

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	CCLR[1:0]		CKEG[1:0]		TPSC[2:0]		
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
2 to 0	TPSC[2:0]*	TRGCNT count clock select	000: TRGCNT counts the internal clock φ 001: TRGCNT counts the internal clock φ/2 010: TRGCNT counts the internal clock φ/4 011: TRGCNT counts the internal clock φ/8 100: TRGCNT counts the internal clock φ/32 101: TRGCNT counts the TCLKA pin input 110: ~~TRGCNT counts the internal clock φ/40~~ Setting prohibited. 111: TRGCNT counts the TCLKB pin input	R/W

2.6 Others

(1) When an external oscillator is used for system clock, each PJ1 pin and PJ0 pin are assigned for OSC1 pin and OSC2 pin, and thus, these pins can not be used for general port or CLKOUT pin.

(2) The description regarding high-speed OCO in H8S/20103,H8S/20203,H8S/20223 Group Hardware manual (Rev.1.00), which is not shown in this document, is not valid.

3. A plan of future

Renesas continues to improve the high-speed OCO to realize the precision of ±1% guarantee.

Renesas will announce again, once the prospect of improvement is confirmed.