To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A610A/E	Rev.	1.00
Title	The spec deletion and usage note about synchronous serial communication unit (SSU)		Information Category	Technical Notification		
Applicable Product	R5S72630P200FP R5S72631P200FP R5S72632P200FP R5S72633P200FP R5S72030W200FP	Lot No. ALL	Reference Document	・SH7263 Group Hardware Manual Rev.1.00 (REJ09B0290-0100) ・SH7203 Group Hardware Manual Rev.1.00 (REJ09B0313-0100)		

We would like to inform you of the following spec deletion and usage note about synchronous serial communication unit (SSU) included in the above-mentioned applicable products.

1. Spec deletion of SSCRL.FCLRM

Following shows spec deletion of bit 7 (FCLRM) in of SS control register L (SSCRL).

Please use this bit as “0” in either case that transmit data registers or receive data registers are accessed by CPU or DMAC.

[Before]

Bit	Bit Name	Initial Value	R/W	Description
7	FCLRM	0	R/W	Flag Clear Mode Selects whether to clear interrupt flags when the register is accessed or when DMAC transfer is completed. When using the DMAC, set this bit to 1. 0: Flags are cleared when the register is accessed 1: Flags are cleared when DMAC transfer is completed

[After]

Bit	Bit Name	Initial Value	R/W	Description
7	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

2. Usage note about slave reception in SSU mode

Following shows the usage note about slave reception in SSU mode.

(However, this note does not apply to simultaneous transmission/reception in SSU mode or in clock synchronous communication mode.)

When continuous slave receptions in SSU mode, SS receive register (SSRDR) needs to be read before next reception is started (i.e. before master device connected outside starts next transmission). If next reception is started before SSRDR is read after receive data full (RDRF) bit in SS status register (SSSR) is set to 1, and then SSRDR is read before one frame of the reception is completed, conflict/incomplete error (CE) bit in SSSR is set to 1 after one frame of the reception is completed. Else if next reception is started before SSRDR is read after RDRF is set to 1, and SSRDR is not read even after one frame of the reception is completed, neither CE bit nor overrun error (ORER) bit in SSSR is set to 1, but the receive data is neglected.