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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A837A/E	Rev.	1.00
Title	SH7786 Address Space Manual Correction		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No. All lots	Reference Document	SH7786 Group User's Manual: Hardware Rev.1.00 Nov 30, 2010 (REJ09B0501-0100)		

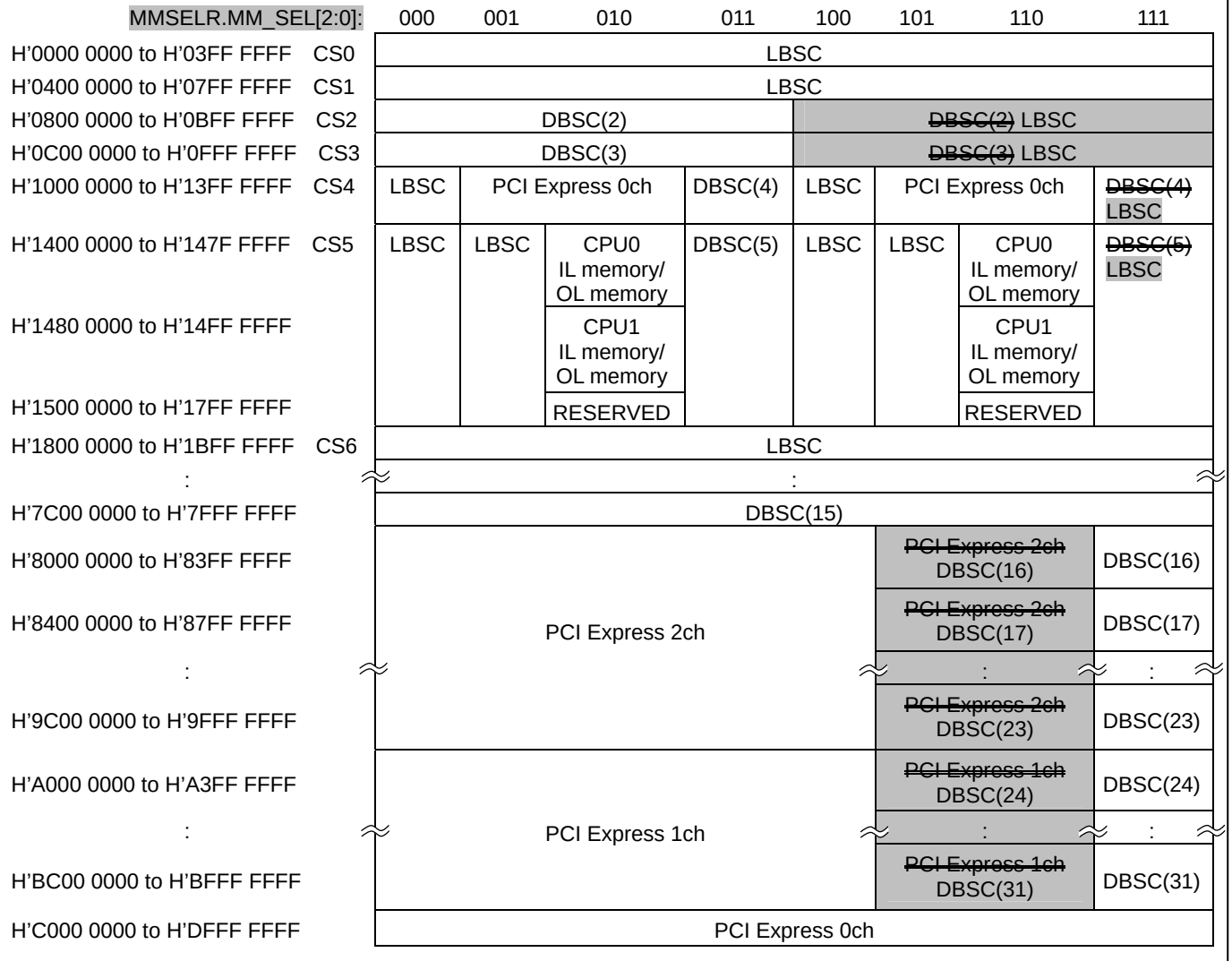
There are some corrections about the SH7786 Address space description in user's manual.

Cancelation line parts (~~abc~~) are deleted and gray parts (abc) are newly added.

[Correction]

1. Section 1.5 Address Map Figure 1.4 SH7786 Address Map

Reference document page 22, Figure 1.4: 1st line, CS2 to CS5 DBSC, space and address after H'8000 0000.



H'E400 0000 to H'E4FF FFFF	Shared Memory*
H'E500 0000 to ~~H'F7FF FFFF~~ H'E7FF FFFF	CPU Internal Modules
H'E800 0000 to H'E87F FFFF	CPU0 IL memory/OL memory
H'E880 0000 to H'E8FF FFFF	CPU1 IL memory/OL memory
H'E900 0000 to H'FBFF FFFF	CPU Internal Modules
H'FC00 0000 to H'FFFF FFFF	Peripheral Modules

Note: * When the secondary cache is used as shared memory, the area from H'E400 0000 to H'E403 FFFF (256 KB) is in RAM.

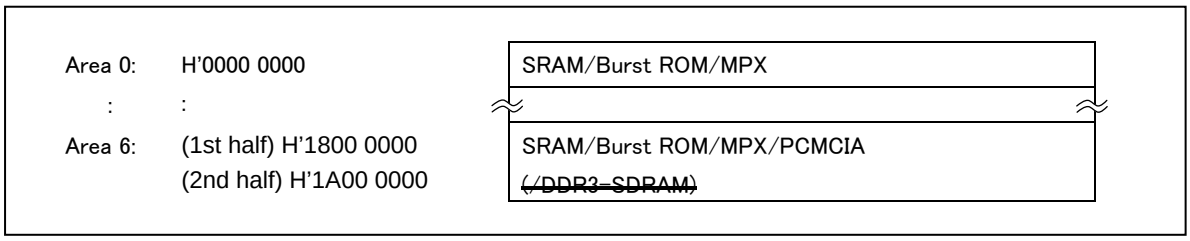
2. Section 11.3 Overview of Areas Table 11.2 LBSC External Memory Space Map

Reference document page 382, Table 11.2: Access Size, Area 2 to 5 DDR3-SDRAM.

Area	External Address	Size	Connectable Memory	Specifiable Bus Width (bits)	Access Size*7
0	H'0000 0000 to H'03FF FFFF	64 Mbytes	SRAM :	8, 16, 32*1 :	8/16/32 bits, 8/16/32 bytes
1	H'0400 0000 to H'07FF FFFF	64 Mbytes	SRAM :	8, 16, 32*2 :	8/16/32 bits, 8/16/32 bytes
2	H'0800 0000 to H'0BFF FFFF	64 Mbytes	: (DDR3-SDRAM) *3	: ~~16,~~ 32*3	8/16/32 bits, 8/16/32 bytes
3	H'0C00 0000 to H'0FFF FFFF	64 Mbytes	: (DDR3-SDRAM) *3	: ~~16,~~ 32*3	8/16/32 bits, 8/16/32 bytes
4	H'1000 0000 to H'13FF FFFF	64 Mbytes	: (DDR3-SDRAM) *3 (PCIEC) *4	: ~~16,~~ 32*3 ~~32~~ –	8/16/32 bits, 8/16/32 bytes
5	H'1400 0000 to H'17FF FFFF	64 Mbytes	: (DDR3-SDRAM) *2 3 (LRAM) *8	: ~~16,~~ 32 –	8/16/32 bits, 8/16/32 bytes
6	H'1800 0000 to H'1BFF FFFF	64 Mbytes	SRAM :	8, 16, 32*2 :	8/16/32 bits, 8/16/32 bytes

3. Section 11.3 Overview of Areas Figure 11.3 Local Bus Memory Space Allocation

Reference document page 384, Figure 11.3: Area 6



- End of Correction -