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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A778A/E	Rev.	1.00
Title	SH7780 FLCTL Manual Correction		Information Category	Technical Notification		
Applicable Product	SH7780 Group	Lot No. All lots	Reference Document	SH7780 Hardware Manual Rev.1.00, Dec.13.2005 (REJ09B0158-0100)		

There are corrections to the SH7780 hardware manual regarding the description of the FLCTL (NAND Flash Memory Controller).

Gray parts are newly added or changed (example: ABC) and cancellation line parts are removed (example: ~~ABC~~).

[Correction]

Reference document 27.3.1 Common Control Register (FLCMNCR) bits 9 and 8 of table (NANDWF and SE) (Page 1027 of 1286) are corrected as follows.

27.3.1 FLCMNCR Description in table (bit 9)

Bit	Bit Name	Initial Value	R/W	Description
9	NANDWF	0	R/W	NAND Wait Insertion Operation 0: Performs address or data input/output in one FCLK cycle (No wait insertion) 1: ~~Performs address or data input/output in two FCLK cycles~~ Setting prohibited
8	~~SE~~ —	0	R/W	~~Spare Area (control code area) Enable bit~~ ~~0: Spare area access enable (can be access the data area and the control code area continuously)~~ ~~1: Spare area access disable~~ ~~In sector access mode, clear this bit to 0.~~ ~~Reserved~~ This bit is always read as 0. The write value should always be 0.

[Note]

For the NANDWF bit, the SH7780 does not have a wait insertion function. When setting to 1 to NANDWF, the operation of the FLCTL becomes unstable and cannot access the memory correctly.

- End of Correction -