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HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	25 January 2001	No.	TN-SH7-295A/E
THEME	SH7751 PCIC arbiter interrupt usage notice		
CLASSIFICATION	☐ Spec change ■ Limitation on Use ☐ Supplement of Documents		
PRODUCTNAME	HD6417751	Lot No.etc.	All
REFERENCE DOCUMENTS	SH7751 Hardware Manual	Rev.	EffectiveDate
		1	From Eternal

1. Usage notice : Error interrupts (target bus timeout interrupt or master bus timeout interrupt) .

1.1 Abstract

SH7751 asserts the specific bit in PCI arbiter interrupt register (PCIAINT), when PCIC, performing as the host with the arbitration function, detects violation of the 16/8 clock rules (the upper limitations of cycles for the target latency and the master data latency) by an external PCI device.

When an external PCI target device violates the limitation of the target latency, bit 12 (TGT_BUSTO) is asserted, and an external PCI master device violates the limitation of the master data latency, bit 11 (MST_BUSTO) is asserted. Then PCIC can generate an error interrupt according to these bits.

In SH7751, it is defined that these limitations of cycles are 1 clock shorter than the PCI2.1 specification.

1.2 Details

If the target latency or the master data latency of an external PCI device are given as following timing (1) or (2). In these cases, although these latencies do not violate the 16/8 clock rules at PCI2.1 specification, SH7751 regards these latencies as violation of the 16/8 clock rules and asserts TGT_BUSTO or MST_BUSTO.

(1) Target latency: SH7751 generates Target Bus Timeout Interrupt (asserting TGT_BUSTO)

An external PCI target device completes the initial data phase of transaction (i.e. the target device asserts TRDY# or PCISTOP#) at 16 clocks from the assertion of PCIFRAME#.

Or an external PCI target device completes a subsequent data phase at 8 clocks from the completion of the previous data phase.

(Refer to Fig.1 and Fig.2)

(2) Master data latency: SH7751 generates Master Bus Timeout Interrupt (asserting MST_BUSTO)

An external PCI master device asserts its IRDY# for the initial data phase at 8 clocks from the assertion of PCIFRAME#.

Or an external PCI master device asserts its IRDY# for a subsequent data phase at 8 clocks from the previous data phase.

(Refer to Fig.3 and Fig.4)

2. Workaround

When the PCIC is operating as the host with the arbitration function and the external PCI device connected to SH7751 which spends full clocks of the 16/8 clock rules for the target latency or the master data latency, the target/master bus timeout interrupt bits (TGT_BUSTO/ MST_BUSTO) in the PCI arbiter interrupt register (PCIAINT) should be masked by the corresponding mask bits in the PCI arbiter interrupt mask register (PCIAINTM).

In the case (1), in order to mask the target bus timeout interrupt, set the bit12 (TGT_BUSTO) in the PCI arbiter interrupt mask register (PCIAINTM) to 0.

In the case (2), in order to mask the master bus timeout interrupt, set the bit11 (MST_BUSTO) in the PCI arbiter interrupt mask register (PCIAINTM) to 0.

It is necessary to take notice that PCIC does not generate the target/master bus timeout interrupt even though PCIC detects the violation of the 16/8 clock rules when the interrupt is masked.

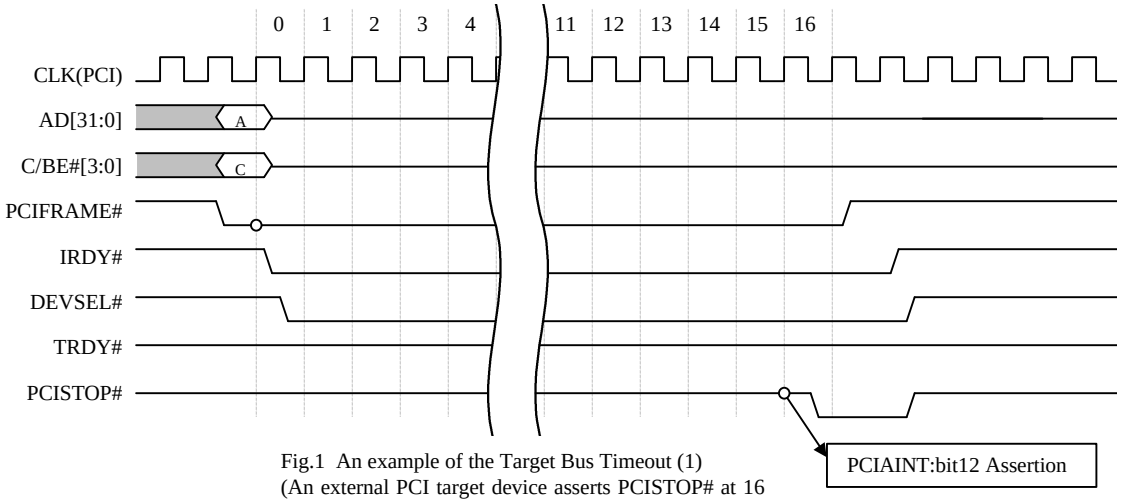

Fig.1 An example of the Target Bus Timeout (1)
(An external PCI target device asserts PCISTOP# at 16 clocks from the assertion of PCIFRAME# for retry termination.)

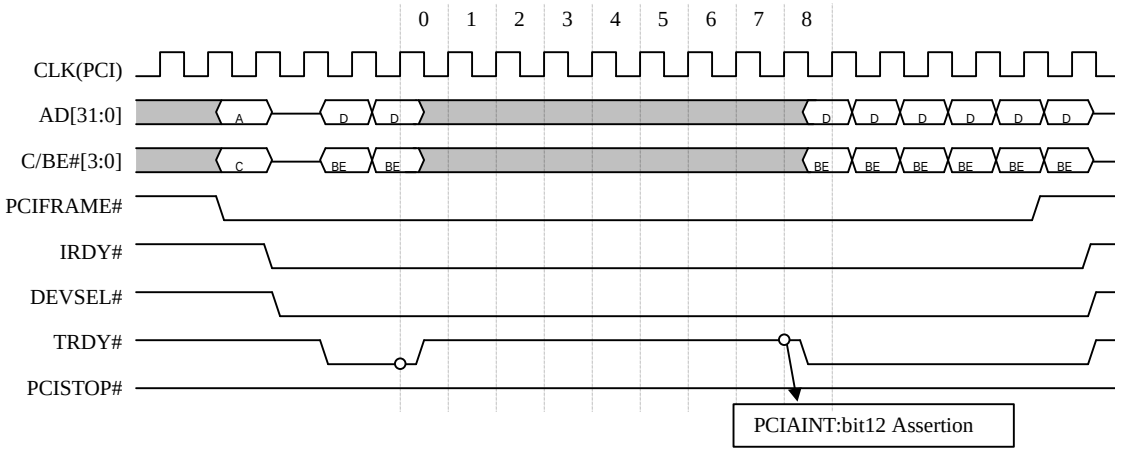

Fig.2 An example of the Target Bus Timeout (2)
(An external PCI target device completes the 3rd data phase at 8 clocks from the completion of the 2nd data.)

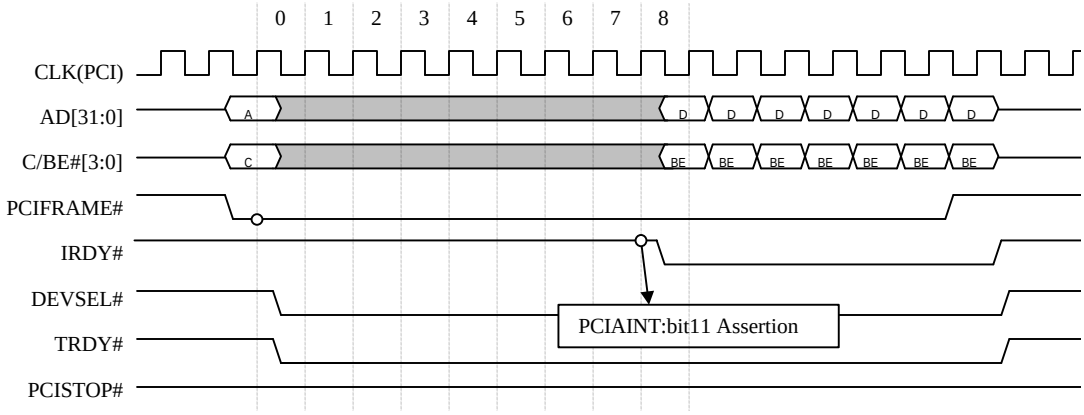

Fig.3 An example of the Master Bus Timeout (1)
(An external PCI master device asserts its IRDY# for initial data phase at 8 clocks from the assertion of PCIFRAME#.)

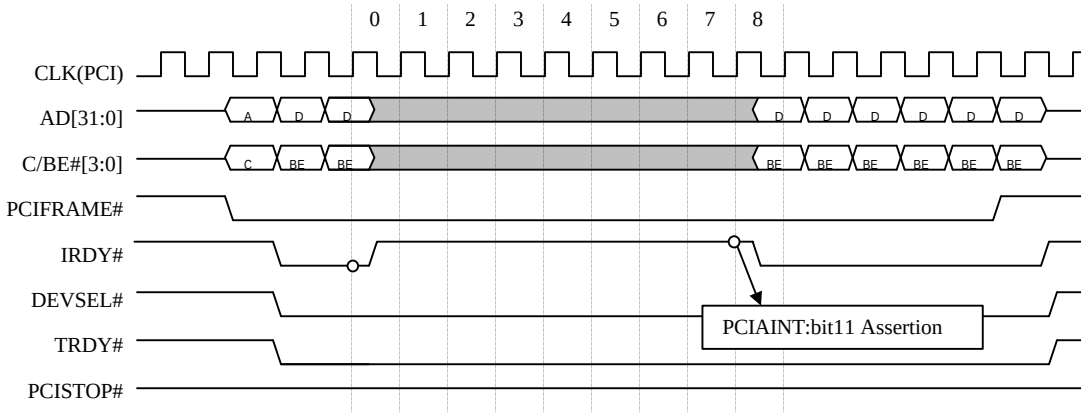

Fig.4 An example of the Master Bus Timeout (2)
(An external PCI master device asserts its IRDY# for the 3rd data phase at 8 clocks from the 2nd data phase.)