## **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU	Document No.	TN-SH7-A880A/E	Rev.	1.00				
Title		750, SH7750S, SH7750R Group Electrical acteristics and Package Dimensions Manual ection			Technical Notification				
Applicable Product		Lot No.							
	SH7750, SH7750S, SH7750R Group	All lots	Reference SH7750, SH7750S, SH7750 Document (R01UH0456EJ0702)			Group			

Regarding SH7750, SH7750S and SH7750R Groups, there are manual corrections about the electrical characteristics

(AC specifications) and package dimensions.

The cancellation line parts are removed (before correction) and the gray parts are added (after correction).

[Correction]

1. Electrical Characteristics Correction

Reference document: "22.3.2 Control Signal Timing"

1) SH7750R (Page 946, Table 22.32 Control Signal Timing, There are five correction parts.)

Max value of bus buffer on time from standby and STATUS delay time are corrected.

		HD6417750R BP240(V) HD6417750R BG240(V) HD6417750R BA240HV		HD6417750R BP200(V) HD6417750R BG200(V) HD6417750R BA240HV*		HD6417750R F240(V)		HD6417750R F200(V)		
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Bus buffer on time from standby	tBON2	_	<del>2</del> 1	_	<del>2</del> 1	-	<del>2</del> 1	_	<del>2</del> 1	tCYC
STATUS0, STATUS1 delay time	tSTD1	-	<del>6</del> 5.3	-	6	-	6	-	6	ns

Note \*: This is the case when the device in use is an HD6417750RBA240HV running at 200MHz.

## 2) SH7750 and SH7750S (Page 947, Table 22.33 Control Signal Timing, There are eleven correction parts.)

Max value of bus buffer on time, bus buffer on time from standby and STATUS delay time are corrected.

			HD6417750 VF128(V)		HD6417750 SVF133(V) HD6417750 SVBT133(V)		HD6417750 F167(V) HD6417750 SF167(V) HD6417750 SF200(V)		HD6417750 BP200M(V) HD6417750 SBP200(V) HD6417750 SBA200V	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Bus buffer on time	tBON1	_	<del>12</del> 15	_	<del>12</del> 15	_	12	_	<del>12</del> 10	ns
Bus buffer on time from standby	tBON2	-	<del>2</del> 1	-	<del>2</del> 1	-	<b></b>	-	<b></b> ≩1	tCYC
STATUS0, STATUS1 delay time	tSTD1	_	<del>6</del> 11	_	<del>6</del> 11	-	<del>6</del> 9	_	<del>6</del> 7	ns

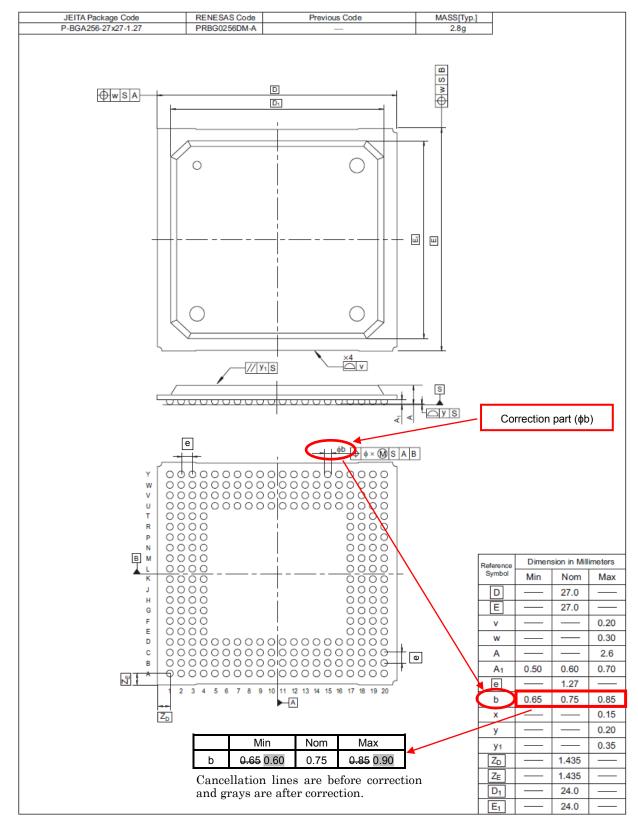


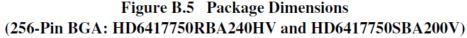
2. Package Dimensions Correction

Reference document: "Appendix B Package Dimensions"

• SH7750R (Page 1027, Figure B.5 Package Dimensions (256-Pin BGA HD6417750RBA240HV and HD6417750R BA200HV))

Ball diameter ( $\phi$ b) specification of the HD6417750RBA240HV and HD6417750SBA200V is corrected as follows.





- End of Correction -

