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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A792B/E	Rev.	2.00
Title	SH7730 Hardware Manual revised		Information Category	Technical Notification		
Applicable Product	SH7730 Group	Lot No. All	Reference Document	SH7730 Group Hardware Manual (REJ09B0359)		

SH7730 Hardware Manual is revised from Rev.2.00. to Rev.3.00

Please refer to main revisions and additions in Rev. 3.00 as shown in the following.

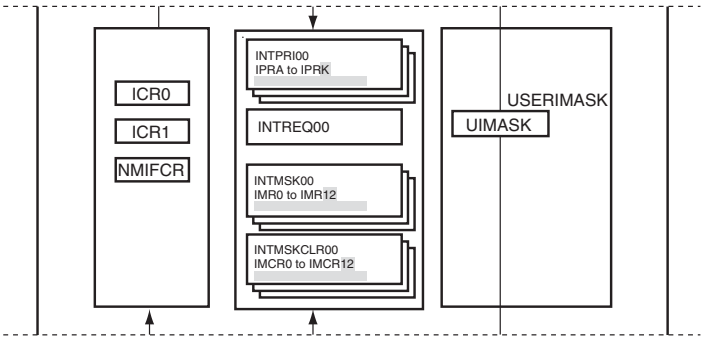
Item	Page	Revision (See Manual for Details)
1.1 Features of This LSI Table 1.1 Features of This LSI	4	Table amended

Item	Features
Bus state controller (BSC)	• SDRAM — Up to two 512-Mbit memory devices or up to one 1-Gbit memory device can be connected — Data bus width: 16 bits or 32 bits — Supports auto-refresh or self-refresh functions — Auto-precharge mode or bank active mode can be selected

	6	Table amended

Item	Features
Clock pulse generator (CPG)	• Clock mode: Input clock selectable from external input (EXTAL) and crystal resonator • Output clock: Bus clock (Bϕ) • Generates four types of system clocks — CPU clock (Iϕ): Maximum 266.7 MHz — SH (SuperHyway) clock (Sϕ): Maximum 133.4 MHz — Bus clock (Bϕ): Maximum 66.7 MHz — Peripheral clock (Pϕ): Maximum 33.4 MHz • Supports power-down mode — Sleep mode — Software standby mode — Module standby mode

7.8.2 Notes on the Unbuffered Write Setting	204	Newly added
8.1 Features Figure 8.1 Configuration of Operand Cache Figure 8.2 Configuration of Instruction Cache	209, 210	Figure title amended

Item	Page	Revision (See Manual for Details)
8.3.1 Read Operation	219	Description amended 4. Cache miss (no write-back) Data is read into the cache line on the way, which is selected to replace, from the physical address space corresponding to the virtual address. When reading data, the read data is returned to the CPU at the point in time when that data arrives in the cache. … 5. Cache miss (with write-back) The tag and data field of the cache line on the way which is selected to replace are saved in the write-back buffer. Then data is read into the cache line on the way which is selected to replace from the physical address space corresponding to the virtual address. When reading data, the read data is returned to the CPU at the point in time when that data arrives in the cache.
8.6.1 IC Address Array Figure 8.5 Memory-Mapped IC Address Array	230	Figure title amended
8.6.2 IC Data Array Figure 8.6 Memory-Mapped IC Data Array	231	Figure title amended
8.6.3 OC Address Array Figure 8.7 Memory-Mapped OC Address Array	233	Figure title amended
8.6.4 OC Data Array Figure 8.8 Memory-Mapped OC Data Array	234	Figure title amended
10.1 Features Figure 10.1 Block Diagram of INTC	246	Figure amended 
10.3.1 Interrupt Control Register 0 (ICR0)	251	Description amended ICR0 sets the input signal detection mode for the external interrupt input pin NMI, IRQ, IRL, and PINT, and indicates the input signal level at the NMI pin.

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10.3.5 Interrupt Request Register 00 (INTREQ00) — 257 — Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ0	0	R/W	Edge detection (IRQnS in ICR1 set to B'00 or B'01) Flag indicating detection of IRQn interrupt • When reading 0: No interrupt request detected 1: Interrupt request detected • When writing 0: The bit is cleared to 0 only if it was previously read as 1. 1: Writing 1 is ignored. Write 1 to the bits other than the bit to be cleared. Note: Write 1 to all bits you do not wish to clear to 0. Level detection (IRQnS in ICR1 set to B'10 or B'11) [LSH in ICR0 set to 1] Indicates whether or not a valid interrupt request is being input to the IRQn pin. • When writing 0: No interrupt request being input 1: Interrupt request being input • Writing to these bits is ignored. [LSH in ICR0 cleared to 0] Flag indicating detection of IRQn interrupt • When reading 0: No interrupt request detected 1: Interrupt request detected • Writing to these bits is ignored.
6	IRQ1	0	R/W	
5	IRQ2	0	R/W	
4	IRQ3	0	R/W	
3	IRQ4	0	R/W	
2	IRQ5	0	R/W	
1	IRQ6	0	R/W	
0	IRQ7	0	R/W	

10.3.5 Interrupt Request Register 00 (INTREQ00) — 258 — Description added

The methods of clearing the bits in this register are as follows.

1. Edge detection

   The interrupt source can be cleared by writing 0 to the corresponding bit after reading it as 1. In this case, write 1 to the bits you do not wish to clear to 0.

2. Level detection (LSH in ICR0 set to 1)

   The corresponding bit is cleared to 0 automatically when the IRQ pin state changes and the interrupt request is negated. It is not necessary to clear the bit in software.

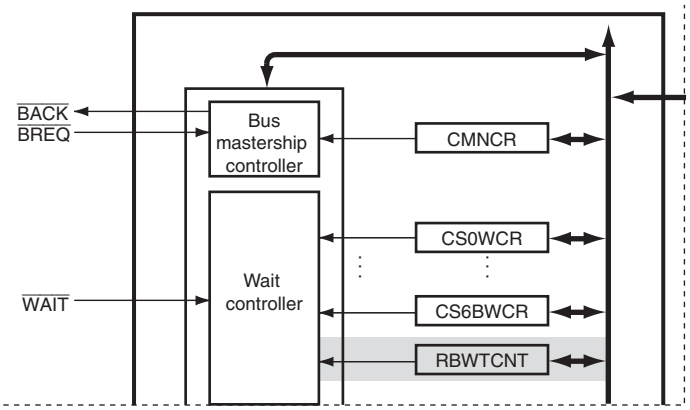
3. Level detection (LSH in ICR0 cleared to 0)

   After the IRQ pin state changes and the interrupt request is negated, write 1 to the corresponding bit in the INTMSK00 register.

10.4.1 NMI Interrupt — 266 — Description amended

The NMI signal is edge-detected. The NMIE bit in ICR0 is used to select either rising or falling edge detection. After the NMIE bit in ICR0 is modified, NMI interrupts are not detected for a maximum of six bus clock cycles.

When the INTMU bit in CPUOPM is set to 1, the SR interrupt mask level (IMASK in SR) is set to 15 automatically when an NMI interrupt is accepted. The reception of an NMI interrupt has no effect on IMASK in SR when the INTMU bit in CPUOPM has been cleared to 0.

Item	Page	Revision (See Manual for Details)
10.4.2 IRQ Interrupts	267	Description amended IRQ interrupts are input on pins IRQ7 to IRQ0. Edge-sensing or level-sensing can be selected by setting the IRQnS bits (n = 0 to 7) in ICR1. When level-sensing is selected, operation differs according to the setting of the LSH bit in ICR0. The initial value of LSH in ICR0 is 0, but it is recommended that it be set to 1 before using the INTC. 1. LSH in ICR0 set to 1 Interrupt requests are not held internally by the INTC. Maintain the state of the IRQ pin until the interrupt is accepted by the CPU and interrupt handling starts. 2. LSH in ICR0 cleared to 0 When the INTC detects an interrupt request from the state of the IRQ pin, it holds the interrupt request in the INTREQ00 register. The value is held in INTREQ00 even if the interrupt request is negated at the IRQ pin before the interrupt is accepted by the CPU. After the request is negated at the IRQ pin, the value of INTREQ00 is cleared either when the CPU accepts an interrupt (which need not be an IRQ interrupt) or when the corresponding bit in the INTMSK00 register is set to 1. Clear the INTREQ00 flag before enabling interrupts by clearing the BL bit or executing the RTE instruction.
11.1 Features	282	Description amended 6. PCMCIA interface • Supports IC memory cards and I/O card interfaces defined in the JEIDA specifications Ver. 4.2 (PCMCIA2.1).
Figure 11.1 Block Diagram of BSC	283	Figure amended 
11.1 Features Figure 11.1 Block Diagram of BSC		Legend added [Legend] RBWTCNT: Reset bus wait counter
11.4 Register Descriptions Table 11.7 Register Configuration	292	Table amended

Name	Abbreviation	R/W	Address	Access Size
SDRAM mode register	SDMR3	W	H'FEC1 5xxx	—
Reset bus wait counter	RBWTCNT	—	—	—

Table 11.8 Register States in Each Operating Mode	293	Table amended

Name	Abbreviation	Power-On Reset	Software Standby	Module Standby	Sleep
SDRAM mode register	SDMR3	—	—	—	—
Reset bus wait counter	RBWTCNT	Initialized	Retained	—	Retained

Item	Page	Revision (See Manual for Details)
11.4.2 CSn Space Bus Control Register (CSnBCR)	298	Table amended

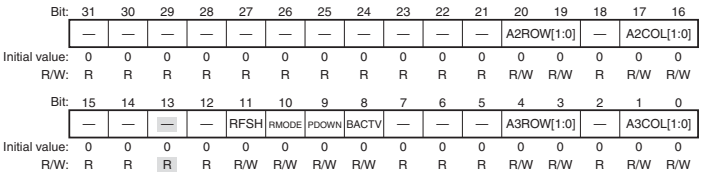
Bit	Bit Name	Initial Value	R/W	Description
30 to 28	IWW[2:0]	011	R/W	Idle Cycles between Write-Read Cycles and Write-Write Cycles These bits specify the number of idle cycles to be inserted after the access to a memory that is connected to the space. The target access cycles are the write-read cycle and write-write cycle. 000: Setting prohibited 001: 1 idle cycle inserted 010: 2 idle cycles inserted 011: 4 idle cycles inserted 100: 6 idle cycles inserted 101: 8 idle cycles inserted 110: 10 idle cycles inserted 111: 12 idle cycles inserted

11.4.3 CSn Space Wait Control Register (CSnWCR) (1) Normal Space and Byte-Selection SRAM • CS2WCR, CS3WCR	306	Table amended

Bit	Bit Name	Initial Value	R/W	Description
23, 22	BW[1:0]	00	R/W	Number of Burst Wait Cycles Specify the number of wait cycles to be inserted to the second and subsequent access cycles in a burst access. Valid for byte-selection SRAM with page mode specified (PMD bit = 1). 00: 0 cycle 01: 1 cycle 10: 2 cycles 11: 3 cycles Note: Bit position is different from that of burst ROM (asynchronous).

11.4.4 Reset Bus Wait Counter (RBWTCNT)	326	Newly added

11.4.5 SDRAM Control Register (SDCR)	327	Figure amended



328 Table amended

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	RFSH	0	R/W	Refresh Control Specifies whether or not the refresh operation of the SDRAM is performed. 0: No refresh 1: Refresh

11.4.6 Refresh Timer Control/Status Register (RTCSR)	330	Table amended

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.

11.4.7 Refresh Timer Counter (RTCNT)	332	Table amended

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.

11.4.8 Refresh Time Constant Register (RTCOR)	333	Table amended

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be H'A55A00.

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>11.5.5 SDRAM Interface
(12) Low-Power SDRAM</td><td>—</td><td>Deleted</td></tr>
<tr><td>11.5.6 Burst ROM (Clock Asynchronous) Interface</td><td>385</td><td>Note added
Note: When using the CS0 space as burst ROM, set CS0BCR and CS0WCR by using a program in a space other than CS0 (on-chip RAM, for example) before accessing the burst ROM.</td></tr>
<tr><td>11.5.8 PCMCIA Interface</td><td>392</td><td>Description amended
With this LSI, if address map (2) is selected using the MAP bit in CMNCR, the PCMCIA interface can be specified in areas 5 and 6. Areas 5 and 6 in the physical space can be used for the IC memory card and I/O card interface defined in the JEIDA specifications version 4.2 (PCMCIA2.1) by specifying the TYPE[3:0] bits of CSnBCR (n = 5B, 6B) to B'0101.</td></tr>
<tr><td>11.6 Usage Notes
(1) Reset</td><td>403</td><td>Description amended
Some flash memories may specify a minimum time from reset release to the first access. To ensure this minimum time, the bus state controller supports a 7-bit counter (RBWTCNT). The counter is cleared to 0 by a power-on reset and it maintains the 0 state during the reset period. After power-on reset, RBWTCNT is counted up synchronously together with CKO and an external access will not be generated until RBWTCNT is counted up to H'007F. At manual reset, RBWTCNT is not cleared.</td></tr>
<tr><td>12.3.7 DMA Channel Control Registers (CHCR_0 to CHCR_5)</td><td>418</td><td>Table amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>23</td><td>DO</td><td>0</td><td>R/W</td><td>DMA Overrun
Selects whether detection takes place at overrun 0 or overrun 1 when DREQ level detection is used. This bit is valid only in CHCR_0 and CHCR_1.
0: Detects DREQ by overrun 0
1: Detects DREQ by overrun 1</td></tr>
</table>
</td></tr>
<tr><td></td><td>420</td><td>Table amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>18</td><td>HIE</td><td>0</td><td>R/W</td><td>Half End Interrupt Enable
Specifies whether an interrupt request is generated to the CPU when the read cycle of the transfer that the number of transfers is decreased to half of the TCR value set before the transfer has ended. If the HIE bit is set to 1, an interrupt request is generated to the CPU when the HE bit is set. To confirm that the half of the transfer has ended, execute a dummy read of the destination space after issuing the SYNCO instruction.
Clear this bit to 0 while reload mode is set. This bit is valid in CHCR_0 to CHCR_3.
0: Half end interrupt disabled
1: Half end interrupt enabled</td></tr>
</table>
</td></tr>
<tr><td>12.3.7 DMA Channel Control Registers (CHCR_0 to CHCR_5)</td><td>423</td><td>Table amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>2</td><td>IE</td><td>0</td><td>R/W</td><td>Interrupt Enable
Specifies whether an interrupt request is generated to the CPU at the end of the final DMA transfer. Setting this bit to 1 generates an interrupt request (DMINT) to the CPU when the TE bit is set to 1 and a read cycle of the final DMA transfer has ended. To confirm that the final transfer has ended, execute a dummy read of the destination space after issuing the SYNCO instruction.
0: Interrupt request disabled.
1: Interrupt request enabled.</td></tr>
</table>
</td></tr>
</table>

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424

Table amended

Bit	Bit Name	Initial Value	R/W	Description
1	TE	0	R/W*	Transfer End Flag The TE bit is set to 1 when DMA transfer count register (TCR) is set to 0 (when the DMAC starts executing the final DMA transfer). The TE bit is not set, if DMA transfer ends due to an NMI interrupt or DMA address error before TCR is cleared to 0, or if DMA transfer is ended by clearing the DE bit and DME bit in DMA operation register (DMAOR). To clear the TE bit, the TE bit should be read as 1, and then, 0 is written to. Even if the DE bit is set to 1 while this bit is set to 1, transfer is not enabled. 0: When DMA transfer is being performed or DMA transfer has been interrupted [Clearing condition]: Write 0 after TE is read as 1 1: TCR = 0 (when the final DMA transfer is being performed or the DMA transfer ends)

12.4.3 DMA Transfer Types

Table 12.8 Supported DMA Transfers

438

Table amended

	Destination				
Source	External Device with DACK	External Memory	Memory-Mapped External Device	On-Chip Peripheral Module	IL Memory
External device with DACK	Not available	Y	Y	Not available	Not available
External memory	Y	Y	Y	Y	Y
Memory-mapped external device	Y	Y	Y	Y	Y
On-chip peripheral module	Not available	Y	Y	Y	Y
IL memory	Not available	Y	Y	Y	Y

Legend added

[Legend]

Y: Transfer is enabled

12.4.3 DMA Transfer Types

Table 12.8 Supported DMA Transfers

Note amended

Note : For on-chip peripheral modules, 16-byte transfer is available only by registers which can be accessed in longword units.

(2) Bus Modes

(a) Cycle-Steal Mode

441

Description amended

- Intermittent mode 16, intermittent mode 64, and intermittent mode 256

In intermittent mode of cycle steal, the DMAC returns the bus mastership to other bus master whenever a unit of transfer (byte, word, longword, 8-byte, 16-byte, or 32-byte unit) is complete. If the next transfer request occurs after that, the DMAC gets the bus mastership from other bus master after waiting for 16, 64, or 256 clocks in Bϕ count.

(3) Relationship between Request Modes and Bus Modes by DMA Transfer Category

Table 12.9 Relationship between Request Modes and Bus Modes by DMA Transfer Category

443

Table amended

Address Mode	Transfer Category	Request Mode	Bus Mode	Transfer Size (Bits)	Usable Channels
Dual	External device with DACK and external memory	External	B/C	1/2/4/8/16/32	0, 1
	External device with DACK and memory-mapped external device	External	B/C	1/2/4/8/16/32	0, 1

12.4.7 DREQ Pin Sampling Timing

449

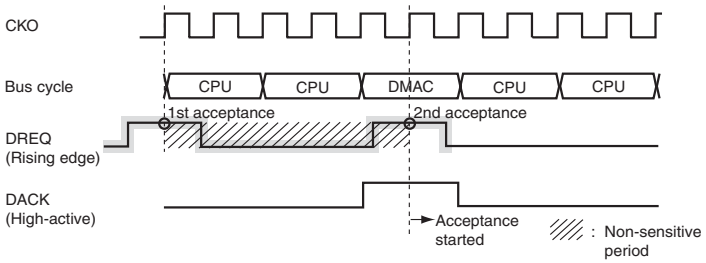
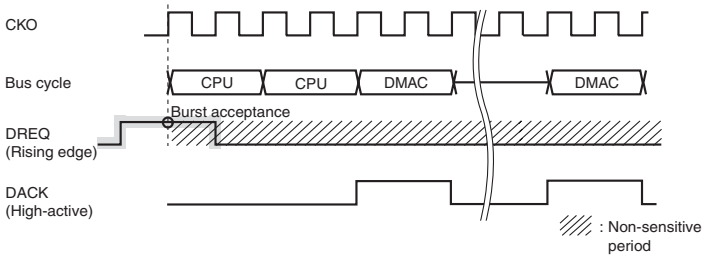
Description added

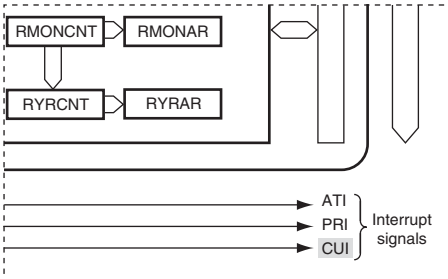
Figures 12.12 to 12.15 show the sample timing of the DREQ input in each bus mode, respectively.

DREQ detection (edge or level detection) sampling takes place at the rising edge of CKO for both assertion and negation.

This means that assertion and negation are possible once every clock cycle, provided the necessary DREQ setup/hold time is guaranteed.

However, there is a non-sensitive period in the case of assertion, and requests are not accepted during this period.

Item	Page	Revision (See Manual for Details)
Figure 12.12 Example of DREQ Input Detection in Cycle Steal Mode Edge Detection		Figure amended 
12.4.7 DREQ Pin Sampling Timing Figure 12.14 Example of DREQ Input Detection in Burst Mode Edge Detection	450	Figure amended 
12.5.5 Notes on Setting of DMA Extended Resource Selectors	453	Newly added
13.1 Features (5) Control Circuit	457	Title and description amended The control circuit controls the clock frequency and sets the power-down modes according to the settings of the MD0 and MD1 pins and the frequency control registers.
(6) Standby Control Circuit (7) Frequency Control Register (FRQCR) (8) Standby Control Register (STBCR) (9) PLL Control Register (PLLCR) (10) IrDA Clock Control Register (IrDACLKCR) (11) Oscillation Settling Time Watch Timer Control Register (OSCWTCR)	—	Deleted
13.4.1 Frequency Control Register (FRQCR)	460	Table amended Bit | Bit Name | Initial Value | R/W | Description 29 | — | Undefined*1 | R | Reserved The write value should always be 0.
13.4.1 Frequency Control Register (FRQCR)	461	Table amended Bit | Bit Name | Initial Value | R/W | Description 19 to 16 | — | Undefined*1 | R | Reserved The write value should always be 0. 7 to 4 | — | Undefined*1 | R | Reserved The write value should always be 0.
13.5.2 Changing the Division Ratio	467	Description amended The division ratio can be changed by overwriting each set of bits for setting the division ratio in FRQCR. The clock changes to the new setting immediately when the contents of FRQCR are changed.

Item	Page	Revision (See Manual for Details)
14.4.3 Software Standby Mode (2) Exit from Software Standby Mode (a) Exit Driven by an Interrupt	487	Description amended When using an externally input clock as the clock source, or when using the crystal resonator as the clock source and the crystal resonator does not stop oscillating in software standby, the occurrence of an NMI, IRQ (edge-detection), PINT, or RTC interrupt causes software standby mode to be canceled and the STATUS0 pin to go low. Note that in order to cancel software standby mode by means of an IRQ (level-detection) interrupt, it is necessary to supply the clock by connecting EXTAL_RTC and XTAL_RTC to the crystal resonator.
16.5.4 PWM Modes	523	Description amended • 0% duty: When periodic register (TPUn_TGRB) is set to the value equal to duty register TGRB + 1
17.1 Features Figure 17.1 RTC Block Diagram	528	Figure amended 
17.3.16 RTC Control Register 1 (RCR1)	546	Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	CF	Undefined	R/W	Carry Flag (CUI) Status flag that indicates that a carry has occurred. CF is set to 1 when a count-up to 64-Hz occurs at the second counter carry or 64-Hz counter read. A count register value read at this time cannot be guaranteed; another read is required. 0: No carry of 64-Hz counter by second counter or 64-Hz counter [Clearing condition] When 0 is written to CF 1: Carry of 64-Hz counter by second counter or 64 Hz counter [Setting condition] When the second counter or 64-Hz counter is read during a carry occurrence by the 64-Hz counter, or 1 is written to CF.
4	CIE	0	R/W	Carry Interrupt Enable Flag (CUI) When the carry flag (CF) is set to 1, the CIE bit enables interrupts. 0: A carry interrupt is not generated when the CF flag is set to 1 1: A carry interrupt is generated when the CF flag is set to 1
3	AIE	0	R/W	Alarm Interrupt Enable Flag (ATI) When the alarm flag (AF) is set to 1, the AIE bit allows interrupts. 0: An alarm interrupt is not generated when the AF flag is set to 1 1: An alarm interrupt is generated when the AF flag is set to 1

	547	Table amended		

Bit	Bit Name	Initial Value	R/W	Description
0	AF	0	R/W	Alarm Flag (ATI) The AF flag is set when the alarm time, which is set by an alarm register (ENB bit in RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, or RYRAR is set to 1), and counter match. 0: Alarm register and counter not match [Clearing condition] When 0 is written to AF. 1: Alarm register and counter match* [Setting condition] When alarm register (only a register with ENB bit set to 1) and counter match Note: * Writing 1 holds previous value.

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17.3.17 RTC Control Register 2 (RCR2) — 548 — Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	PEF	0	R/W	Periodic Interrupt Flag (PRI) Indicates interrupt generation with the period designated by the PES[2:0] bits. When set to 1, PEF generates periodic interrupts. 0: Interrupts not generated with the period designated by bits PES[2:0]. [Clearing condition] When 0 is written to PEF 1: Interrupts generated with the period designated by bits PES[2:0]. [Setting condition] When an interrupt is generated with the period designated by bits PES[2:0] or when 1 is written to the PEF flag
6 to 4	PES[2:0]	000	R/W	Interrupt Enable Flags (PRI) These bits specify the periodic interrupt. 000: No periodic interrupts generated 001: Periodic interrupt generated every 1/256 second 010: Periodic interrupt generated every 1/64 second 011: Periodic interrupt generated every 1/16 second 100: Periodic interrupt generated every 1/4 second 101: Periodic interrupt generated every 1/2 second 110: Periodic interrupt generated every 1 second 111: Periodic interrupt generated every 2 seconds
3	—	1	—	Reserved This bit is always read as 1. The write value should always be 1.

20.3.2 I^2C Bus Control Register 2 (ICCR2) — 589 — Table amended

Bit	Bit Name	Initial Value	R/W	Description
1	IICRST	0	R/W	IIC Control Part Reset Resets the control part except for I^2C registers. If the device hangs because of a problem such as a communication failure during I^2C bus operation, bits BC2 to BC0 in the ICMR register of the IIC and the internal circuits of the IIC can be reset by setting the IICRST bit to 1.

20.3.5 I^2C Bus Status Register (ICSR) — 595 — Table amended

Bit	Bit Name	Initial Value	R/W	Description
3	STOP	0	R/W	Stop Condition Detection Flag [Clearing condition] • When 0 is written in STOP after reading STOP = 1 [Setting conditions] • In master mode, when a stop condition is detected after frame transfer • In slave mode, when STOP condition is detected after the first byte slave address, next to detection of start condition, accords with the address set in SAR.

20.6 Bit Synchronous Circuit — 616 — Figure replaced

Figure 20.18 Bit Synchronous Circuit Timing

Table 20.6 Time for Monitoring SCL — 617 — Table amended

CKS3	CKS2	Time for Monitoring SCL*1
1	0	39 tpcyc*2
	1	87 tpcyc*2

20.7.3 Notes on master receive mode — 618 — Newly added

20.7.4 Note on Setting ACKBT in Master Receive Mode — 618 — Newly added

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20.7.5 Issuance of Stop Condition and Repeated Start Condition — 618 — Newly added

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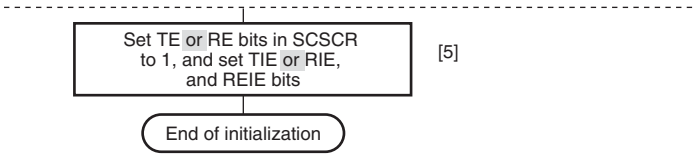
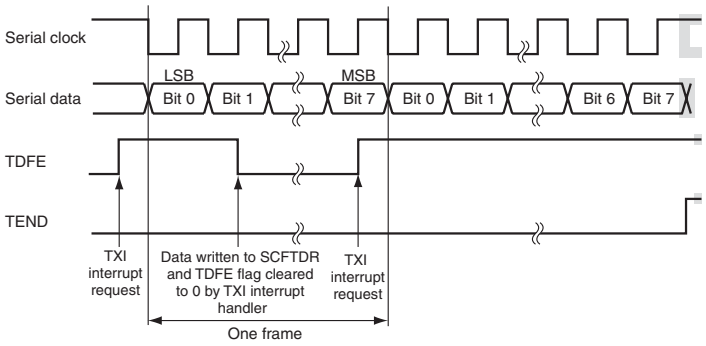
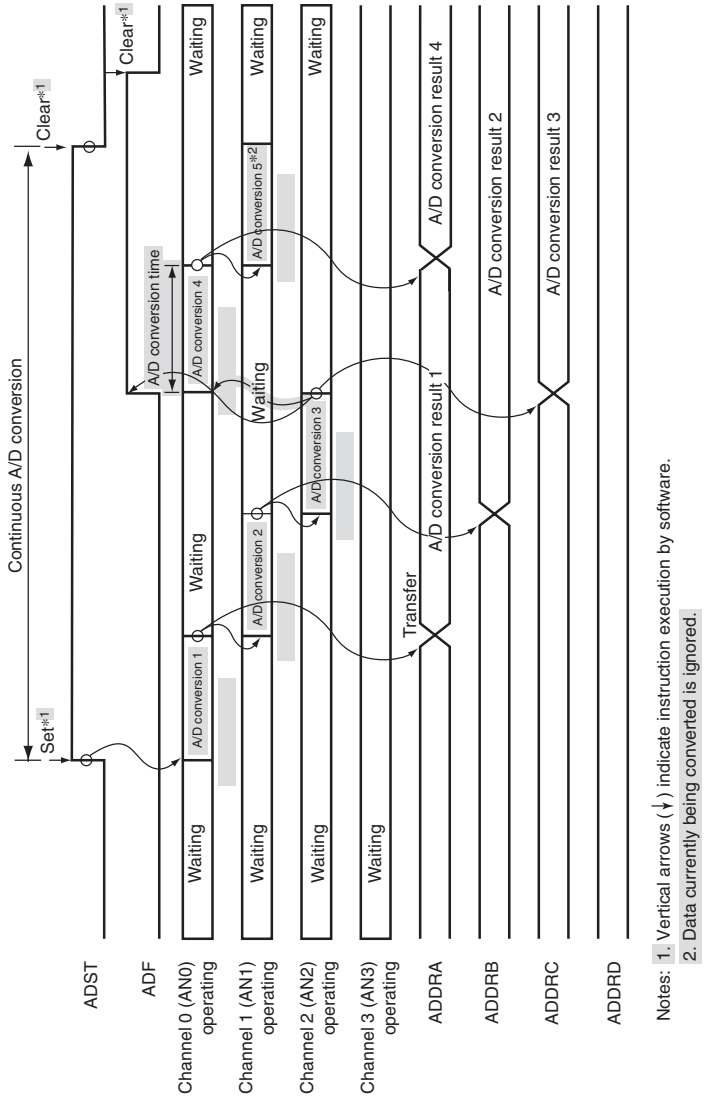
21.5.2 Note on Interrupting Transfers — 671 — Newly added

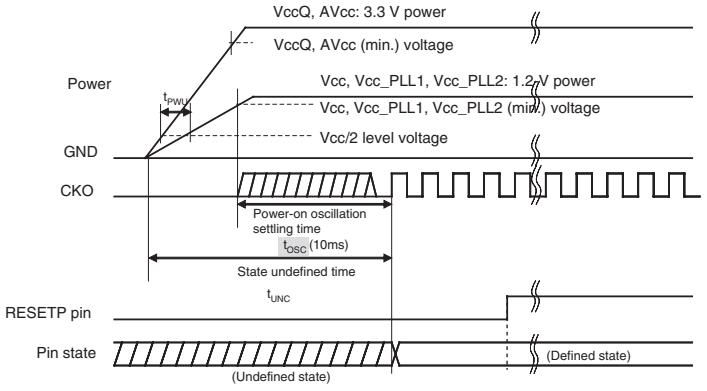
Item	Page	Revision (See Manual for Details)
22.4.3 Operation in Clock Synchronous Mode Figure 22.12 Sample Flowchart for SCIF Initialization	716	Figure amended 
Figure 22.14 Example of SCIF Transmit Operation	718	Figure amended 
22.5 SCIF Interrupt Sources and DMAC	722	Description amended Clearing the RIE bit to 0 and setting the REIE bit to 1 in SCSCR generates only an ERI and BRI interrupt request without generating an RXI interrupt request.
23.1 Features	727	Description amended • The direct memory access controller (DMAC) can be activated to transfer data in the event of transmit-FIFO-data-empty and receive-FIFO-data-full.
23.3.6 Serial Control Register (SCASCR)	741	Table amended **Bit** / **Bit Name** / **Initial Value** / **R/W** / **Description** 1, 0 / CKE[1:0] / 00 / R/W / Clock Enable These bits select the SCIFA clock source and should be set before selecting the SCIFA operating mode by SCASMR. • Asynchronous mode 00: Internal clock; SCK pin used as input pin (input signal is ignored)*1 01: Setting prohibited 10: External clock, SCK pin used for clock input*3 11: Setting prohibited • Synchronous mode 00: Setting prohibited 01: Internal clock, SCK pin used for synchronous clock output*2 10: External clock, SCK pin used for clock input 11: Setting prohibited Notes: 1. When the data sampling is done using on-chip baud rate generator, CKE[1:0] should be set to 00. 2. The output clock frequency is the same as the bit rate. 3. Input a clock with a frequency 8 times the bit rate. The sampling rate is fixed at 1/16. When the external clock is not input, CKE[1:0] should be set to 00.
23.4.2 Asynchronous Mode	758	Description amended • Clock source: Internal clock/external clock — Internal clock: SCIFA operates using the on-chip baud rate generator — External clock: The sampling rate is fixed at 1/16, so a clock with a frequency 8 times the bit rate is required. (The internal baud rate generator should not be used.)
23.4.3 Serial Operation (2) Clock	760	Description amended Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK pin can be selected as the SCIFA's serial clock, according to the setting of the CKE bit in SCASCR. The sampling rate is fixed at 1/16 when an external clock is input on the SCK pin, so input a clock with a frequency 8 times the bit rate.

Item	Page	Revision (See Manual for Details)
(3) Transmitting and Receiving Data (b) Serial Data Transmission	764	Description amended — Transmit data stop function When the value of the SCATDSR register and the number of transmit data bytes match, transmit operation stops. Setting the TSIE bit (interrupt enable bit) allows the generation of an interrupt.
23.5 Interrupt Sources and DMAC	781	Description amended Activating the DMAC and transferring data can be performed by the transmit-FIFO-data-empty interrupt request . The DMAC transfer request is automatically cleared when the number of data bytes written to SCAFTDR by the DMAC is increased more than that of setting transmit triggers. … The activation of DMAC and generation of an interrupt are not executed at the same time by the same source. To activate the DMAC, set the interrupt enable bit (TIE or RIE) corresponding to the generated interrupt source and the appropriate transfer enable bit (TDRQE or RDRQE) to 1.
Table 23.7 SCIFA Interrupt Sources	782	Table amended **Interrupt Source** — **DMAC Activation** Interrupt initiated by receive error (ER), break (BRK), data ready (DR), or transmit data stop (TSF) — Not possible Interrupt initiated by receive FIFO data full flag (RDF) or transmit FIFO data empty (TDFE) — Possible Notes deleted
23.6 Usage Notes (5) Limitation on Simultaneous Transmission and Reception in Clock-Synchronous Mode	784	Newly added
26.3.2 A/D Control/Status Registers (ADCSR)	873	Table amended **Bit** — **Bit Name** — **Initial Value** — **R/W** — **Description** 11, 10 — TRGE[1:0] — 00 — R/W — Trigger Enable Enables or disables A/D conversion by external trigger input. 00: Disables A/D conversion by external trigger input 01: Reserved (setting prohibited) 10: Reserved (setting prohibited) 11: A/D conversion is started at the falling edge of A/D conversion trigger pin (ADTRG)

Item	Page	Revision (See Manual for Details)
26.4.3 Scan Mode Figure 26.4 Example of A/D Converter Operation (Scan Mode, Channels AN0 to AN2 Selected)	880	Figure amended

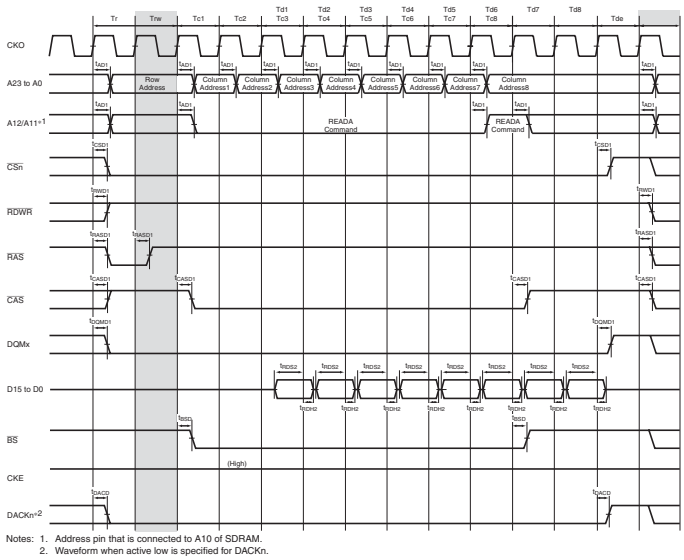


33.2 Power-On and Power-Off Order (1) Order of turning on 1.2 V power (V_{CC}, V_{CC}_PLL1, and V_{CC}_PLL2) and 3.3 V power ($V_{CC}Q$, AV_{CC})	1068	Figure amended



33.4 AC Characteristics Table 33.6 Maximum Operating Frequencies	1074	Table amended

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating frequency	CPU clock (Iϕ)	f	24	—	266.7	MHz	266 MHz version
			24	—	200		200 MHz version
	SH clock (Sϕ)		24	—	133.4		
	Bus clock (Bϕ)		24	—	66.7		
	Peripheral clock (Pϕ)		8	—	33.4		
	PLL circuit output clock		75	—	266.7		266 MHz version
			75	—	200		200 MHz version

Item	Page	Revision (See Manual for Details)
33.4.6 SDRAM Timing Figure 33.19 Burst Read Bus Cycle of SDRAM (Single Read × 8) (Auto Precharge Mode, CAS Latency 2, TRCD = 2 Cycles, TRP = 1 Cycle)	1092	Figure amended  Notes: 1. Address pin that is connected to A10 of SDRAM. 2. Waveform when active low is specified for DACKn.