HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	1 December 2000	No.	TN-SH7-254B/E
THEME	SH7729/SH7709A usage notice about DACK when using DMAC(No.1)		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	■ Limitation on Use	
PRODUCT NAME	HD6417709A, SH7729		
REFERENCE DOCUMENTS	SH7709A Hardware manual SH7729 Hardware manual	Effective Date From	Eternity

HD6417729 and HD6417709A have followed usage notice.
This technical update is the revised version of 'TN-SH7-254A/E : SH7729/SH7709A usage notice about DACK when using DMAC'.

1. condition and phenomenon

- Using PCMCIA (A5(6)PCM in BCR is set to 1)
- A5(6)TEH[2:0] in PCR is set to other than 3'b000
- A PCMCIA bus cycle followed by a DMA bus cycle with asserting DACK

On above conditions, DACK0/1 may be asserted incorrectly at the PCMCIA bus cycle.

2. work around

Either (1) , (2) or (3) is work around.

(1) Please don't use PCMCIA and DMAC at the same time.
(2) When you use PCMCIA and D MAC at the same time, please set A5(6)TEH[2:0] to 3'b000.
(3) Please fix DACK to high during PCMCIA bus cycle.

3. Note

Even if DACK is asserted incorrectly,DMA bus cycle never be generated while the incorrect DACK signal is asserted.

Following is the difference from the previous 'TN-SH7-254A/E'.
(1) '3'b001 of A5(6)TEH[2:0] setting' is removed from the workaround because this setting may have same problem.
(2) 'To use dual address mode for DMA channel 0/1 and specify DACK output in write cycle by AM bit of CHCR register' is removed from the workaround because this setting may have same problem.