To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A632A/E	Rev.	1.00
Title	SH7619 SIOF Defect		Information Category	Technical Notification		
Applicable Product	R4S76190B125BGV,R4S76190N125BGV, R4S76190W125BGV,R4S76190D125BGV, R4S76190B125BG,R4S76190N125BG, R4S76190W125BG,R4S76190D125BG	Lot No. All lots	Reference Document	SH-2 SH7619 Group Hardware Manual (REJ09B0237-0500)		

We would like to inform valued customers of the in using SH7619 Group as follows.

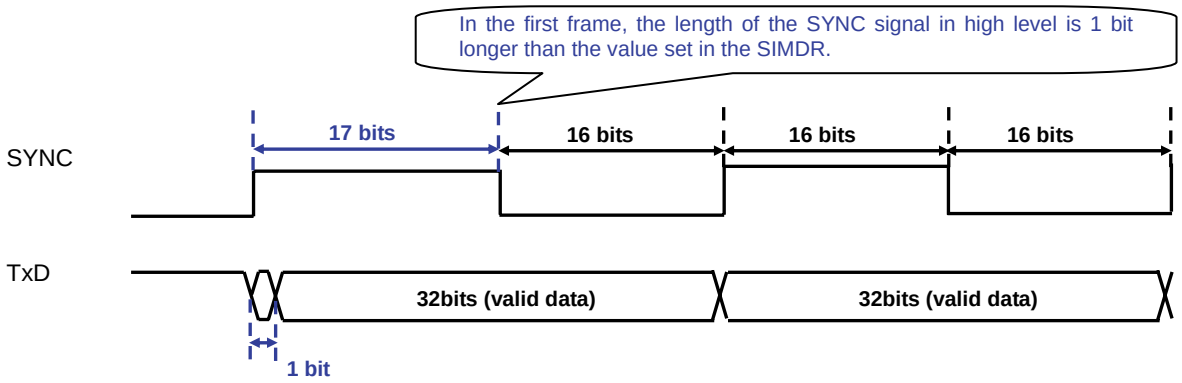
-Note-

There are two types of defect in data transmission operation in SH7619 Group. Please refer following details.

1. Defect in Frame Synchronous Signal (SYNC) Length

1.1. Phenomena

With the SIOF Master Mode 2, in some case, the length of the SYNC signal in high level error occurs by changing the SYNC signal output condition from disabled (the FSE bit = 0) to enabled (the FSE bit = 1). In the above case, the SYNC signal rises before the correct timing and the length of the signal in high level will be 1 bit longer in the first frame than the value set in the SIMDR, whereas the error DOES NOT occur after second frame.



(Example): With the SIOF Master Mode 2, Frame Length = 32 bits

1.2. Defect prevention

*Please take following procedures (1) or (2).

(1) In the case of setting a data, please write a dummy data for the first frame and the valid data for other frames into the transmit FIFO, and set the destination stations to discard the data in the first frame.

(2) In the use of this product, please make your system composition that works correctly even in the case that the length of the SYNC signal will be 1 bit longer.

2. Resume Data Transmission with the SIOF Master Mode

2.1. Defect data transmission

With the SIOF master mode, in some case, the data is NOT transmitted correctly when the transmission operation is resumed after stopping the previous transmission operation by setting '0' to the TXE bit.

2.1. Cause of the Defect

After the transmission, the SIOF will be reset and initialized by setting the TXE bit in the SICTR to '0' with the SIOF master mode 1/2. However, if that SIOF fails to be reset, the transmission will resume without the transmission module initialized and the defect mentioned above will occur.

2.3. Defect prevention

Please change the setting of SCK temporarily to make reset the modules using the CK clock surely, specifically, whenever the TXE bit or the RXE bit in SICTR is set to '0', please take the procedures as follows;

(1) Set the Pϕ as the master clock source.
(Set the MSSEL bit in SISCR to '1' (master clock = Pϕ).)

(2) Set the master clock division ratio according with the count value of the prescalar of the baud rate generator as ×1/1.
(Set the bits BRPS[4:0] in SISCR to '0000' (as the master clock frequency ×1/1)).

(3) Set the frequency division ratio for the output stage of the baud rate generator as ×1/1.
(Set the bits BRDV[2:0] in SISCR to '111' (as the prescalar out put frequency ×1/1).)

(4) Reset the transmission/reception operation.
(Set the TXRST bit (or RXST bit) in the SICTR to '1' (reset).)

(5) Set the value of SISCR for transmission/reception again, before start of next transmission/reception.

Please refer following details for the transmission/reception operation by CPU.

Transmission/Reception Operation in Master Mode (Example of Reception and Full-Duplex Transmission by the CPU with TDMAE=0)

No	Flow chart	SIOF Settings	SIOF Operation
1	Start ↓ Set SIMDR,SISCR,SITDAR,SIRDAR, SICDAR, and SIFCTR	Set operating mode, serial clock, slot positions for transmit/receive data, slot position for control data, and FIFO request threshold value	
2	↓ Set the SCKE bit in SICTR to 1	Set operation start for baud rate generator	[Note] Serial clock will not be output from the pin until communication is actually started.
3	↓ Set the FSE bit in SICTR to 1	Set the start for frame synchronous signal output	
4	↓ Set the TXE and RXE bit in SICTR to 1	Enable transmission and reception	[Note] Communication is actually started after SITDR has been written.
4	↓ TDREQ=1? No ↓ Yes		
5	Set the SITDR register		
6	↓ Transmit SITDR from SIOFTXD synchronously with SIOFSYNC	Set transmit data	Transmission and reception are carried out simultaneously (Even when transmission is not necessary, dummy transmission must be performed. The output of dummy transmission can be masked by setting the pin function).
7	↓ RDREQ=1？ No ↓ Yes		
8	Read SIRDR register	Read receive data	
9	↓ Transfer complete? No ↓ Yes		Transmission and reception are carried out simultaneously, please check the TFEMP bit in SISTR (the transmit FIFO is empty?) and build a waiting loop to check the communication finished.
10	Clear the TXE bit and RXE bit in SICTR to 0 ↓	Disable transmission	End transmission
11	Clear the FSE bit in SICTR to 0 ↓	To be prepared for the transmission/reception that is resumed later, set the FSE bit to '0' to synchronize the frame in this LSI.	
12	Set the MSSEL bit in SISCR to 1 ↓ Set the BPRS to 00000 and the BRDV to 111in SISCR ↓ Apply a pulse to bits TxRST and RxRST in the SICTR (input 0→1→0) ↓ Set the SISCR to set the baud rate and the master clock source again	To be prepared for the transmission/reception that is resumed later, initialize inside the baud rate generator.	
13	↓ Change communication mode？ No → END ↓ Yes	If communication is not to be resumed (branching to No), no further setting is needed. To return to the same communication mode, go back to setting of FSE at step 3 of this flowchart.	
14	With FSE=0,TXE=0,and RXE=0 held, start setting other bits.	Go on to 'Start' of the corresponding flowchart.	

Transmission Operation in Master Mode (Example of Half-Duplex Transmission by the CPU with TDMAE=0)

No	Flow chart	SIOF Settings	SIOF Operation
1	Start ↓ Set SIMDR, SISCR, SITDAR, SIRDAR SICDAR, and SIFCTR	Set operating mode, serial clock, slot positions for transmit/receive data, slot position for control data, and FIFO request threshold value	
2	↓ Set the SCKE bit to 1 in SICTR	Set operation start for baud rate generator	[Note] Serial clock will not be output from the pin until communication is actually started.
3	↓ Set the FSE bit in SICTR to 1	Set the start for frame synchronous signal output	
4	↓ Set the TXE, and RXE bit in SICTR to 1	Enable transmission and reception	[Note] Communication is actually started after SITDR has been written.
5	↓ TDREQ=1? No ↓ Yes		
6	Set SITDR register	Set transmit data	
7	↓ Transmit SITDR from SIOFTXD synchronously with SIOFSYNC		Transmission
8	↓ Transfer complete? No ↓ Yes	*Please check the TFEMP bit in SISTR (the transmit FIFO is empty?) and build a waiting loop to check the communication finished.	
9	Clear the TXE bit in SICTR to 0	Disable transmission	End of transmission
10	↓ Clear the FSE bit in SICTR to 0 ↓	To be prepared for the transmission/reception that is resumed later, set the FSE bit to '0' to synchronize the frame in this LSI.	
11	Set the MSSEL bit in SISCR to 1 ↓ Set the BPRS to 00000 and the BRDV to 111 in SISCR ↓ Apply a pulse to bits TxRST and RxRST in the SICTR (input 0→1→0) ↓ Set the SISCR register to set the baud rate and the master clock source again	To be prepared for the transmission/reception that is resumed later, initialize inside the baud rate generator.	
12	↓ Change communication mode ? No → END ↓ Yes	If communication is not to be resumed (branching to No), no further setting is needed. To return to the same communication mode, go back to setting of FSE at step 3 of this flowchart.	
13	With FSE=0,TXE=0,and RXE=0 held, start setting other bits.	Go on to 'Start' of the corresponding flowchart.	