To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A578B/E	Rev.	2.00
Title	SH7619, PHY registers adjusting waveform		Information Category	Technical Notificaion		
Applicable Product	R4S76190B125BGV,R4S76190N125BGV, R4S76190W125BGV,R4S76190D125BGV, R4S76190B125BG,R4S76190N125BG, R4S76190W125BG,R4S76190D125BG	Lot No. All lots	Reference Document	SH-2 SH7619 Group Hardware Manual (REJ09B0237-0400 Rev.4.00)		

We would like to inform valued customers of the usage of SH7619 Group as follows.

-Note-

In the Ethernet PHY module on SH7619 have test registers to adjust the Tx100 slope waveforms of differential outputs. Of course you could use with its initial value, but we would discloser it to make designing substrates easier in your site.

Please refer following details.

Adjustment of Tx100 waveform.

The on-chip PHY module of this LSI has below adjustment registers as SMI registers.

The waveform in the Tx100 mode could be adjustable with them.

Basically those registers are protected from overwriting easily.

Please change them in the manner of the following descriptions.

REGISTER 20 : A register for changing operating modes.

REGISTER 23 : A register for adjusting waveform.

(The numbers of registers are counted in decimal.)

The meanings of the values to be written to REGISTER 23.

Bit	Bit name	Initial value	R/W	Description
15	Reserved	1	RO	Reserved bit. The write value should always be 1.
14-9	Reserved	0	RO	Reserved bit. The write value should always be 0.
8	D1CMP	1	RW	Adjustment to the end of the slopes (from the half to maximum amplitude) 00: Three steps up 01: Two steps up 10: One step up 11: Regular
7	D0CMP	1	RW	
6	D2A	1	RW	Adjustment of amplitudes. 000: Amp 4 stp+ 001: Amp 3 stp+ 010: Amp 2 stp+ 011: Amp 1 stp+ 100: Regular 101: Amp 1 stp- 110: Amp 2 stp- 111: Amp 3 stp-
5	D1A	0	RW	
4	D0A	0	RW	
3	DASL	1	RW	Adjustment to the beginning of the slopes (from the 0v to half amplitude) 00: One step up 01: One step down 10: Regular 11: Two steps down
2	DBSL	0	RW	
1-0	Reserved	0	RO	Reserved bit. The write value should always be 0.

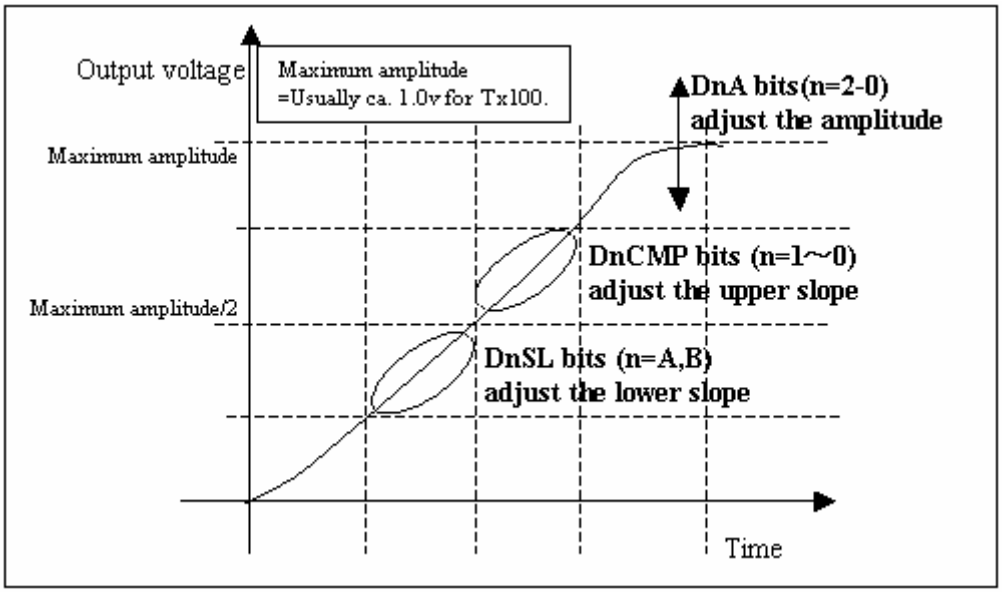

Figure. The roles of corresponding bits. (ex. for rising waveform)

Controlling a slope in 4 steps.

USAGE (example)

Please write SMI registers in the following manner.

Step.	Corresponding register	Write value	Description
1	0	H'2100	Set to Tx100. (You can skip this step, if auto negotiation result is Tx100 full duplex or Tx100 half duplex.)
2	20	H'0000	Start the sequence of operating mode to write registers.
3	20	H'0000	Start the sequence of operating mode to write registers.(continuation)
4	20	H'0400	Start the sequence of operating mode to write registers.(continuation)
5	20	H'0000	Start the sequence of operating mode to write registers.(continuation)
6	20	H'0400	Complete the sequence of the operating mode to write registers.
7	23	H'xxxx	Set the adjustment value. (The initial value H'81C8 is the regular one)
8	20	H'4416	Enables the adjustment value. (Just write this value)
9	20	H'0000	Exit from the operating mode to write registers. (Back to the normal mode)

NOTE:

The adjustments above are initialized with an auto-negotiation and a reset of PHY module (a reset of entire LSI, also).

-End of Report-