To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPD

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A547A/E	Rev.	1.0
Title	SH7615/SH7616 specification change of internal Ethernet controller.		Information Category	Technical Notification		
Applicable Product	HD6417615 HD6417616	Lot No. ALL	Reference Document	SH7615 Hardware manual (ADE-602-198 Rev.1.0) SH7616 Hardware manual (ADE-602-243 Rev.1.0)		

The specification of Ethernet controller direct memory access controller (E-DMAC) of SH7615/SH7616 is corrected as follows.

[Phenomenon]

(1) Without regard to a value of TRSCER, the value of EtherC/E-DMAC status register (Bit12 to 8, Bit5 to 0) will be reflected to the TFE/RFE bit of a descriptor.

(2) Transmit abort Detect (TFS8)/ Receive abort Detect (RFS8)/ Transmit Frame Error (TFE)/ Receive Frame Error (RFE) are set when error status is set to the descriptor concerned.

Therefore, the specification about the Transmit/receive status copy enable register(TRSCER) and descriptor are changed as follows.

[Specification change]

1. Transmit/receive status copy enable register (TRSCER)

<Before>

Bit:	31	30	29	. . .	19	18	17	16
	-	-	-	. . .	-	-	-	-
Initial value:	0	0	0	. . .	0	0	0	0
R/W:	R	R	R	. . .	R	R	R	R

Bit:	15	14	13	12	11	10	9	8
	-	-	-	ITFCE	CNDCE	DLCCE	CDCE	TROCE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	RMAFCE	-	RFARCE*1	RRFCE	RTLFCE	RTSFCE	PRECE	CERFCE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R or R/W *1	R/W	R/W	R/W	R/W	R/W

*1- Only HD6417616 is effective. HD6417615 is Reserved bit.

<After>

Bit:	31	30	29	. . .	19	18	17	16
	-	-	-	. . .	-	-	-	-
Initial value:	0	0	0	. . .	0	0	0	0
R/W:	R	R	R	. . .	R	R	R	R

Bit:	15	14	13	12	11	10	9	8
	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	RMAFCE	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R

Bits 31 to 8- Reserved: These bits are always read as 0. The write value should always be 0.

Bit 7- Multicast Address Frame Receive(RMAF) Bit Copy Enable(RMAFCE)

Bit 7: RMAFCE

0	Enables the RMAF bit status to be indicated in the RFS7 bit in the receive descriptor.
1	Disables occurrence of corresponding source to be indicated in the RFS7 bit in the receive descriptor.

Bits 6 to 0- Reserved: These bits are always read as 0. The write value should always be 0.

2. Descriptor

<Before>

Transmit Descriptor 0 (TD0)

Bit27– Transmit Frame Error (TFE) : Indicates that one or other bit of the transmit frame status indicated by bits 26 to 0 is set. Whether or not the transmit frame status information is copied into this bit is specified by the transmit/receive status copy enable register.

Bits26 to 0 – Transmit Frame Status 26 to 0 (TFS26 to TFS0) : These bits indicate the error status during frame transmission.

- TFS26 to TFS5– Reserved
- TFS4– Illegal Transmit Frame (corresponds to ITF bit in EESR)
- TFS3– Carrier Not Detect (corresponds to CND bit in EESR)
- TFS2– Detect Loss of Carrier (corresponds to DLC bit in EESR)
- TFS1– Collision Detect (corresponds to CD bit in EESR)
- TFS0–Transmit Retry Over (corresponds to TRO bit in EESR)

Receive Descriptor 0 (RD0)

Bit27– Receive Frame Error (RFE) : Indicates that one or other bit of the receive frame status indicated by bits 26 to 0 is set. Whether or not the receive frame status information is copied into this bit is specified by the transmit/receive status copy enable register.

Bits26 to 0 – Receive Frame Status 26 to 0 (RFS26 to RFS0) : These bits indicate the error status during frame reception.

- RFS26 to RFS10– Reserved

· RFS9– Receive FIFO Overflow (corresponds to RMAF bit in EESR)

· RFS8– Reserved

· RFS7– Receive Multicast Address Frame (corresponds to RMAF bit in EESR)

· RFS6– Reserved *1

· RFS5– Receive Frame Discard Request Assertion (corresponds to RFAR bit in EESR) *1

· RFS4– Receive Residual-Bit Frame (corresponds to RRF bit in EESR)

· RFS3– Receive Too-Long Frame (corresponds to RTLF bit in EESR)

· RFS2– Receive Too-Short Frame (corresponds to RTSF bit in EESR)

· RFS1– PHY-LSI Receive Error (corresponds to PRE bit in EESR)

· RFS0– CRC Error on Received Frame (corresponds to CERF bit in EESR)

*1- Only HD6417616 is effective. HD6417615 is Reserved bit.

<After>

Transmit Descriptor 0 (TD0)

Bit27– Transmit Frame Error (TFE) : Indicates that one or other bit of the transmit frame status indicated by bits 26 to 0 is set.

Bits26 to 0 – Transmit Frame Status 26 to 0 (TFS26 to TFS0) : These bits indicate the error status during frame transmission.

· TFS26 to TFS9 Reserved

· TFS8– Transmit Abort Detect

Note: This bit is set to 1 when any of Transmit Frame Status bits 4 to 0 is set.
When this bit is set, the Transmit Frame Error bit (bit 27: TFE) is set to 1.

· TFS7 to TFS5– Reserved

· TFS4– Illegal Transmit Frame (corresponds to ITF bit in EESR)

· TFS3– Carrier Not Detect (corresponds to CND bit in EESR)

· TFS2– Detect Loss of Carrier (corresponds to DLC bit in EESR)

· TFS1– Collision Detect (corresponds to CD bit in EESR)

· TFS0–Transmit Retry Over (corresponds to TRO bit in EESR)

Receive Descriptor 0 (RD0)

Bit27– Receive Frame Error (RFE) : Indicates that one or other bit of the receive frame status indicated by bits 26 to 0 is set. Whether or not the multicast address frame receive information, which is part of the frame status, is copied into this bit is specified by the transmit/receive status copy enable register.

Bits26 to 0 – Receive Frame Status 26 to 0 (RFS26 to RFS0) : These bits indicate the error status during frame reception.

· RFS26 to RFS10– Reserved

· RFS9– Receive FIFO Overflow (corresponds to RFOF bit in EESR)

· RFS8– Receive Abort Detect

Note: This bit is set to 1 when any of Receive Frame Status bit 9, bit 7, bits 4 to 0 is set.

When this bit is set, the Receive Frame Error bit (bit 27: RFE) is set to 1.

· RFS7– Receive Multicast Address Frame (corresponds to RMAF bit in EESR)

· RFS6– Reserved *1

· RFS5– Receive Frame Discard Request Assertion (corresponds to RFAR bit in EESR) *1

· RFS4– Receive Residual-Bit Frame (corresponds to RRF bit in EESR)

· RFS3– Receive Too-Long Frame (corresponds to RTLF bit in EESR)

· RFS2– Receive Too-Short Frame (corresponds to RTSF bit in EESR)

· RFS1– PHY-LSI Receive Error (corresponds to PRE bit in EESR)

· RFS0– CRC Error on Received Frame (corresponds to CERF bit in EESR)

*1- Only HD6417616 is effective. HD6417615 is Reserved bit.